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Volume 9 Number 9 September 2007

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COM 4	RS-232	NA	RS-232
COM 5	RS-232/422/285	NA	NA
COM 6	RS-422/485/TTL	NA	NA
LPT1	0	0	1
EIDE	2	2	1
USB	2	6	2
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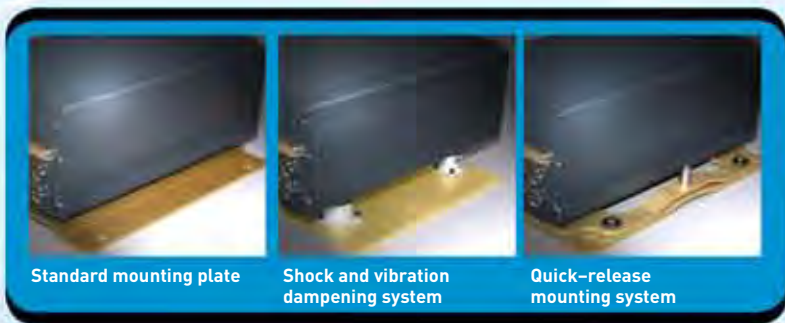
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COTS (kots), *n.* 1. Commercial off-the-shelf. Terminology popularized in 1994 within U.S. DoD by SECDEF Wm. Perry's "Perry Memo" that changed military industry purchasing and design guidelines, making Mil-Specs acceptable only by waiver. COTS is generally defined for technology, goods and services as: a) using commercial business practices and specifications, b) not developed under government funding, c) offered for sale to the general market, d) still must meet the program ORD. 2. Commercial business practices include the accepted practice of customer-paid minor modification to standard COTS products to meet the customer's unique requirements.

—**Ant.** When applied to the procurement of electronics for the U.S. Military, COTS is a procurement philosophy and does not imply commercial, office environment or any other durability grade. *E.g., rad-hard components designed and offered for sale to the general market are COTS if they were developed by the company and not under government funding.*

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Two F-15E Strike Eagles and a B-2 Spirit bomber fly in formation over an airbase. Raytheon has been contracted to develop a new Ku-band AESA (Active Electronically Scanned Array) antenna for the B-2 radar to avoid interference with commercial satellite systems. Installation of the new antenna on the B-2 fleet is to be completed by 2010.



Courtesy: U.S. Air Force Tech. Sgt. Cacilio Ricardo

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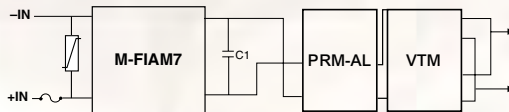
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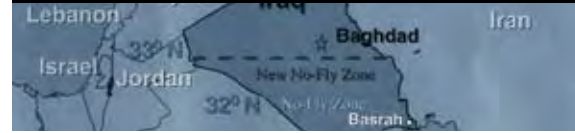
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Publisher's Notebook



Military Embedded Industry EKG

Is it just me or are there others of you out there who just think that the government has got everything screwed up right now? Please don't e-mail me your opinion with respect to which party or branch of the government is at fault. They're all at fault. We have too few elected officials whose prime concern is good government rather than personal or party success. Whether it's groups or individuals, I get the feeling everyone is sitting back and doing virtually nothing except positioning for the 2008 election—unless you consider a full-time effort to make the opposition look bad as doing what we elected them to do. Well government can't just sit and tread water for another year. It has to do something other than pretending to stick a finger in the dike every time something hits the fan. Now that I've gotten that off my chest I can go on.

The embedded electronics market has gone through cycles of feast and famine—like the pendulum in a clock. By that I don't mean the aggregate growth of the market. I mean where the money goes. Sometimes the money goes to the big guys with unquestioning value for what the government gets. Sometimes it goes to the smaller guys because the big guys can't get funding for their overhead and design effort. We know where the pendulum has been recently, and there has been a lot of talk about altering that position through oversight and reform. I guess being in favor or opposed to this type of change depends on whether you're working for one of the big or small guys. It's very callous to state that, in the end, the military doesn't really care—but that's true. The top-end uniformed guys still get to play footsie with the big guys one way or the other, basically interviewing for jobs after retirement.

These cycles that our industry experiences remind me of watching a heart monitor connected to a patient. I envision it like a saw-toothed wave on the monitor with roughly a two-year rhythm riding on a steadily growing baseline. Each wave has varying amplitude peaks and troughs influenced by economics, politics and world events. And every two years I write saying, "Just hang in there." "Give it a little time and it will get better," and it usually does. I probably repeated that song again somewhere in mid-2006. Now, instead of the slow anticipated increase, I think our market is experiencing arrhythmia. RFQs, orders and deliveries all seem to be in some form of chaos. And if your company isn't experiencing any of this consider yourself lucky. I'm not saying the market is bad, it's just all over the place.

Prior to re-organizing themselves for an anticipated tightening of controls and oversight by Congress, the big guys are trying to squeeze every dollar that they can out of the government. Congress, who said they were going to increase control and oversight,

continues to talk and achieve nothing. The Administration and the DoD keep using smoke and mirrors along with a shell game to fund the troops while Congress tries to walk a razor blade saying it supports the troops but won't fund the Administration's war. The end result is that funding for the troops has to come from somewhere. And like little electric shocks out of the blue, our industry gets hit. Many of the larger programs also get hit but then may get re-invigorated because they are part of the political bartering between legislators, with that re-invigoration eventually trickling down to us.

I don't see how this can continue for another year. But I also don't see anything on the horizon that will alter the current course. Only a major external event, acting like a defibrillator, will have the ability to get things back to normal prior to the next election. I know this sounds negative and that's not my intent. There are many programs and companies that are doing well right now; but there are some that because of the "luck of the program draw" are experiencing difficulties. It goes back to the embedded military marketing strategy that says, if you want to succeed in this market you need to be in it for the long haul and have your foot in many different programs. For all you stock guys, the analogy is clear: you want to run a fund, not gamble on a few potential high rollers.

Whether you're looking into or out of the military embedded cardiac ward, it can be very difficult to focus on the fact that the trend line is still moving up. But it is. The heyday of the big guys expanding internally to capture and justify more DoD dollars will slowly start to come to an end. More money will shift to the smaller suppliers with no change in the net result to the military. I know that last sentence will get me a lot of e-mails from people working in, or closely with, the big guys, saying I don't know what I'm talking about and that words like those only jeopardize our troops. In fact, they don't. The bottom line is still "product to fit the mission," no matter who supplies it. Wherever it comes from and whoever is responsible for deciding what to put in the deliverable, must ensure that it does just that.

The government needs to cut back on the fat, stop all the stress and exercise its available alternative options. Where have I heard that before?

Pete Yeatman, Publisher
COTS Journal

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The Inside Track

L-3 BT Fuze Chosen to Supply the 105 mm Cartridge for the Stryker MGS

The U.S. Army Joint Munitions and Lethality Life Cycle Management Command, Picatinny Arsenal, NJ has awarded BT Fuze Products, a division of L-3 Communications, a firm-fixed-price contract to produce M467A1 training cartridges for the Stryker Mobile Gun System (Figure 1).

The 105 mm M467A1 cartridge consists of an inert projectile with a tracer that is a ballistic match to the 105 mm M393A3 HEP "Bunker Buster" cartridge. The Army's Brigade Combat Team utilizes the M467A1 cartridge for target practice training purposes. This award is the division's fourth annual option award under the current contract. BT Fuze is the systems contractor for both the 105mm M467A1 and M393A3 cartridges and also developed and manufactures the related M578A1 fuze.

The Mobile Gun System configuration carries a General



Figure 1

The Stryker Mobile Gun System configuration carries a 105 mm tank cannon in a low-profile, fully stabilized, "shoot on the move" turret. The vehicle operates with the latest C4ISR equipment as well as detectors for nuclear, biological and chemical weapons.

Dynamics 105 mm tank cannon in a low-profile, fully stabilized, "shoot on the move" turret. Its armor protects the three-soldier crew from machine gun bullets, mortar and artillery fragments on the battlefield. The Stryker Mobile Gun System can fire 18 rounds of 105 mm main gun ammunition; 400 rounds of .50 caliber ammu-

munition; and 3,400 rounds of 7.62 mm ammunition. It operates with the latest C4ISR equipment as well as detectors for nuclear, biological and chemical weapons.

L-3 BT Fuze Products
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[www.l-3com.com/btфуze].

VMETRO Acquires Micro Memory

VMETRO and Micro Memory announced that VMETRO has acquired 100% of the shares of privately held Micro Memory. According to VMETRO, the acquisition of Micro Memory is an element of VMETRO's growth strategy that increases VMETRO's capabilities and product offerings in existing and new markets. The addition of Micro Memory improves VMETRO's capabilities to serve existing defense and aerospace customers and further increases

VMETRO's market diversification. This combines VMETRO's worldwide presence—its two European design centers and its strong sales and marketing infrastructure with Micro Memory's technology, its U.S. customer base and its U.S. design center.

Micro Memory's real-time embedded system products are expected to add breadth and depth to VMETRO's embedded Digital Signal Processing (DSP) and high-performance data recording offerings. VMETRO also said that it will leverage Micro

Memory's U.S.-based operations, which will enable selling into programs where U.S. Engineering and Manufacturing facilities are strongly favored—especially those programs that involve sensitive information subject to United States International Traffic in Arms Regulations (ITAR), which limit the involvement of non-U.S. personnel.

Micro Memory
Chatsworth, CA.
(818) 998-0070.
[www.micromemory.com].

VMETRO
Houston, TX.
(281) 584-0728.
[www.vmetro.com].

Endevco Sensors Serve Monitoring Needs on Shuttle Main Engines

Endevco provided advanced accelerometers for new main engine controllers used in the latest Space Shuttle launch. On August 8, a trio of main engines provided by Pratt & Whitney Rocketdyne lifted the space shuttle Endeavour (Figure 2) into orbit and on its way to the International Space Station. The Space Shuttle Main Engines (SSMEs) were fitted with new controllers, using Endevco model 7704M7 vibration sen-



Figure 2

Space Shuttle Endeavour lifts off from Kennedy Space Center on August 8, the Endeavor's first launch since 2002. The STS-118's mission delivered a new truss segment to the International Space Station.

sors, to actively monitor engine health and performance.

All three Pratt & Whitney Rocketdyne SSMEs, the world's only reusable rocket engines, carried the new Advanced Health Management System (AHMS) controllers, which monitor engine turbopump vibration and can automatically shut down an engine if conditions warrant. The controllers also track a history of key performance parameters. This

was the first mission in which all three controllers were in active mode and enabled to prompt actions in the engine systems if unacceptable vibration levels were detected during the eight and one-half minute firing of the engines during launch. The AHMS controller improves flight safety by offering near-instant and automatic response to potential problems in the event they occur.

The Endeveco model 7704 series Isoshear piezoelectric accelerometers are designed to be extremely stable and insensitive to environmental inputs such as base bending and thermal transients. This accelerometer series has been tested in a radiation environment up to 108 rads without performance degradation and features Endeveco's Piezite Type P-8 crystal element, operating in shear mode.

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[www.endeveco.com].

DataPath Wins Contract to Support CENTCOM Sat Comm Hubs

DataPath, a provider of satellite and wireless communications networks around the world, has been awarded a \$7.8 million contract to provide field services for a critical network of 32 DataPath Deployable Ku Band Earth Terminals in the U.S. Central Command (CENTCOM) area of responsibility in Southwest Asia. The contracting authority is the Communications-Electronics Command in Fort Monmouth, N.J.

Program Manager WIN-T's Commercial SATCOM Terminal Program awarded the delivery order through the Worldwide Satellite Systems contract. Under the delivery order, 69 DataPath field service representatives will

provide operations and maintenance services for an initial six-month base period. The agreement provides the option for additional six-month awards to be made in the following three years. With all options exercised, the total value of the program could exceed \$50 million. In addition to the DKET network, DataPath specializes in designing, installing and managing other critical communications networks such as the U.S. Army's Joint Network Node and the U.S. Marines' Support Wide Area Network.

DataPath

Duluth, GA.

(678) 597-0300.

[www.datapath.com].

BAE Systems Selects GE Fanuc to Participate in Taranis UAV Program

GE Fanuc Embedded Systems announced that the company's RT4 had been selected by BAE Systems for deployment within the UK Ministry of Defence's "Taranis" technology demonstrator program to support the development of a world



Figure 3

The Taranis UAV program (artist's rendering shown) will explore and demonstrate how emerging technologies and systems can deliver battle-winning capabilities for the UK armed forces. Ground testing of Taranis is expected to take place in early 2009 with the first flight trials taking place in 2010.

class UAV (Figure 3). The RT4 was designed and manufactured by Radstone Embedded Computing at its Towcester, England headquarters; Radstone was recently acquired by GE Fanuc Embedded Systems.

The RT4 is a small form factor CompactPCI-based rugged compute node with four conduction-cooled 3U slots, one of which is pre-loaded with the IMP2A single board computer. It features a high integrity bonded section chassis construction to provide exceptional strength, while the I/O connector panel and backplane are formed as a single, removable assembly for ease of maintenance.

BAE Systems, together with Rolls-Royce, Smiths Aerospace and QinetiQ, will work alongside the UK Ministry of Defence military staff and scientists to develop and fly Taranis. Named after the Celtic god of thunder, Taranis will explore and demonstrate how emerging technologies and systems can deliver battle-winning capabilities for the UK armed forces. Ground testing of Taranis is expected to take place in early 2009 with the first flight trials taking place in 2010.

GE Fanuc Embedded Systems

Charlottesville, VA.

(800) 368-2738.

[www.gefanucembedded.com].

Quantum3D Imaging Gear Tapped for Navy P-3C Trainer System

L-3 Communications Link Simulation and Training (L-3 Link) has selected Quantum3D Independence IDX 2500 ER Image Generator Solutions as part of the upgrades that L-3 Link is performing on the P-3C Tactical Operational Readiness Trainer (TORT) for the U.S. Navy. The P-3C TORT supports training for the entire crew of the P-3C

Orion (Figure 4), which is the primary long-range anti-submarine warfare patrol aircraft for the U.S. Navy. The upgrade provides enhanced fidelity visual and sensor simulation systems that enable P-3C flight crews to train using the complete functionality of the aircraft's sensor systems, and then communicate that mission critical data to other aircraft or command centers. The P-3C TORT upgrades are scheduled for delivery during 2007.



Figure 4

The Lockheed P-3 Orion is a maritime patrol aircraft of the U.S.—and other militaries around the world—used primarily for maritime patrol.

The Quantum3D IDX 2500 ER IG Solutions provided to L-3 Link for the P-3C TORT upgrades provide correlated high-resolution Out-the-Window (OTW) visual and high-fidelity sensor simulation channels that include infrared and visual capabilities that simulate the combinations of Day TV and IR sensors used in the P-3C. The IDX 2500 ER sensor simulation capabilities employ QUEST (Quantum3D Enhanced Sensor Simulation Technology), which combines Quantum3D embedded hardware/software technologies to provide high-fidelity physics-based sensor simulation that maintains 16 bits of dynamic range from the at-aperture rendering through post-processed output.

Quantum3D

San Jose, CA.

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[www.quantum3d.com].

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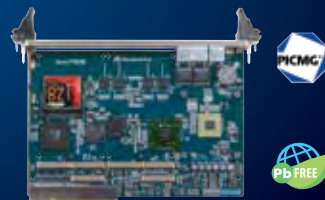


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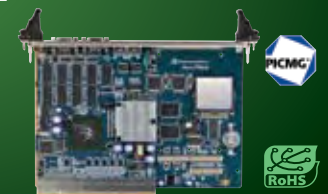
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Special Feature

Nano and High-Density Computing

System Integration Fuels Nano and High-Density Computing

Two embedded trends—nanocomputing and high-density computing—are shaping up as heavyweight champs in terms of their importance to advanced military applications.

Jeff Child
Editor-in-Chief

Highly integrated “nanocomputing” solutions will enable a whole new level of autonomy and mission flexibility for military systems ranging from mini-UAVs to battlefield sensors to ground robots. At the other extreme, many of today’s advanced military programs—in particular unmanned air and ground vehicles—are hungry for high-density embedded computing. The more processing of data and decision making that can be performed on board the UAV itself rather than performed via a communication link with the ground, the more efficiently the craft can be used. Although both of these technology areas—high-density computing and nanocomputing—are fueled by the ongoing magic of semiconductor integration, the issues and challenges they face are quite different from one another.

The definition of the term nanocomputing varies depending on who you talk to. Researchers go so far as to define it as computing on an atomic scale—using



Figure 1

Advances in nanocomputing will result in greater autonomy and longer mission life for systems like this Class I UAV. Shown here, a soldier is preparing the UAV for takeoff during a Future Combat Systems demonstration.

the magnetic orientation of individual atoms as a method to store data. But in the military market—and the embedded computing realm in general—nanocomputing represents more of a technology direction. It’s the trend toward integrating the most computing power possible into the smallest space possible, while requiring the least power possible.

Advances in semiconductor integration enable that trend. The article “Non-Volatile SRAM Ignites Memory Architecture Rethink” on page 26 in this section, for example, explains how the emergence of nvSRAM lets system designers use a single memory device type for both volatile and non-volatile memory storage. Within that scope, military system designers, in contrast to consumer device uses for nanocomputing, still want some degree of modularity—and standardization—in their nanocomputing subsystems.

Longer, More Autonomous Tactical UAV Missions

An example of a military system that’s expected to enjoy direct benefits from advancements in nanocomputing is the Class I Unmanned Aerial Vehicle (UAV) (Figure 1), which is part of the Army’s Future Combat Systems program. The Class I UAV’s role is to provide the dismounted soldier with Reconnaissance, Surveillance and Target Acquisition (RSTA). Estimated to weigh less than 41 pounds, the air vehicle operates in complex urban and wooded terrains with a vertical take-off and landing capability. The UAV uses autonomous flight and navigation, but will interact with the network and soldier to dynamically update routes and target in-



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formation. In the case of the Class I UAV, advances in nanocomputing will result in greater autonomy and longer mission life for the system.

Among the growing crop of vendors specializing in ultra small form-factor embedded computing is Gumstix. This summer Gumstix has launched the third generation of its gumstick-shaped SBC line. The size of a stick of gum, Gumstix are highly functional open source Linux miniature computers. Sporting the Marvell (formerly Intel) PXA270 processor, clocked at up to 600 MHz, the Verdex SBC (Figure 2) integrates up to 128 Mbytes of RAM and 32 Mbytes of flash memory soldered on board. Other enhancements over previous Gumstix SBCs include support for USB host interfaces, inputs for CCD (charge-coupled device) cameras and better power management. Also available is an option for on-board Bluetooth, complete with antenna connector. The Verdex maintains the 3.2 x 0.8 x 3.2-inch (80 x 20 x 8 mm) of Gumstix's earlier SBC generations.

Middleware software vendor PrismTech integrated its Spectra Operating Environment (OE) on the Gumstix family of small form-factor computers. The implementation provides a complete Software Communications Architecture (SCA) software defined radio (SDR) solution on the Gumstix, arguably the world's smallest full-function computer. The low SWaP (size, weight and power) requirements of the Spectra OE solution make standards-based SDRs a viable and cost-effective approach for a large range of small form-factor device requirements within both military and commercial markets.

Nanocomputing Gets Standard Form-Factor

Standards-based form-factors have long been the preference among military system designers. Given the long development cycles typical in defense programs, it helps to be able to design to standard that allows technology upgrades and a variety of vendor sources. Unfortunately, among small nanocomputing-level products there's very little commonality or standardization. Bucking

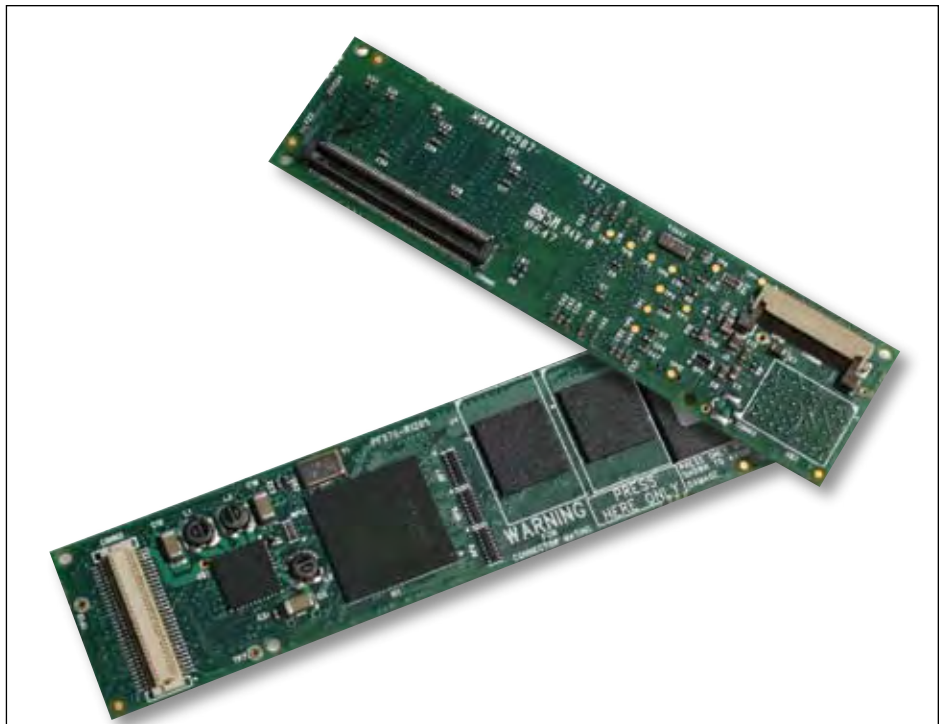


Figure 2

Gumstix's third generation of its gumstick-shaped SBC line is the 600 MHz Marvell PXA270 processor. Clocked at up to 600 MHz, the new Verdex SBC integrates up to 128 Mbytes of RAM and 32 Mbytes of flash memory soldered on board. Other enhancements over previous Gumstix SBCs include support for USB host interfaces.

that trend, in July Kontron announced a new footprint variant of the popular Computer-On-Modules (COMs) standard: nanoETXexpress.

The nanoETXexpress specification is targeted to provide extremely power-saving COMs with mid- to high-performance x86 technology on a footprint that is a mere 55 mm x 84 mm. That's 39 percent of the original COM Express module Basic form-factor. This new COM form-factor follows the PICMG COM Express standard and will be 100 percent compliant with the COM.0 Type 1 connector. The locations of the identically mapped pin-outs will also be 100 percent COM.0 compliant. The goal of the nanoETXexpress specification is to build PCIe-based COMs on the smallest possible form-factor. The specification and documentation for nanoETXexpress will be available under a non-disclosure agreement this fall. Kontron plans to launch its first nanoETXexpress-based COM in Q2 2008.

Performance the Priority in High-Density Computing

While size and power are priorities in nanocomputing, at the other end of the embedded computing spectrum—high-density computing—the primary focus is computing muscle. High levels of compute density are critical to advanced programs such as UAVs, battlefield visualization gear for vehicles and ground soldiers. The article “High-Density Computing Fuels Fusion of Embedded Visual Information” on page 20 in this section discusses how small, lightweight, integrated visual computing systems are enabling military solutions that convert raw data and process sensor input to create true information fusion.

For UAV payloads of the future, the trend is toward fusing data and tasking UAVs to only transmit data that's been processed and narrowed down to critical information. Enabling this boost in embedded compute density is the advance of



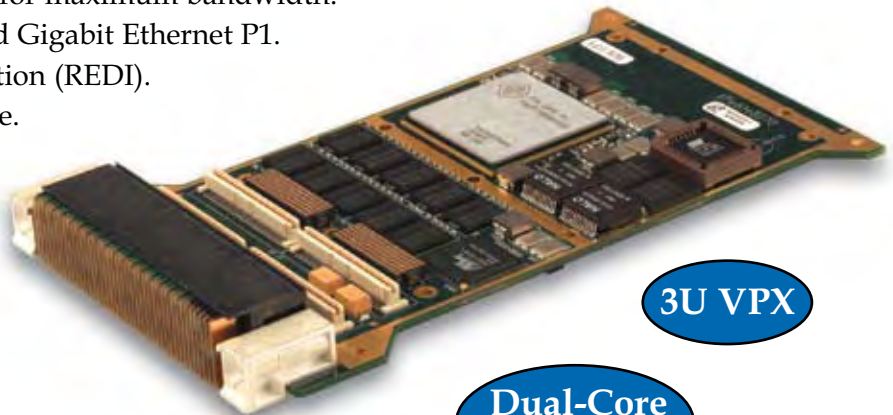
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Figure 3

Targeting mainly networked land-mobile vehicles such as Humvees, Mercury's most compute-dense system is the PowerBlock 200. Mercury's first rugged device designed with the Cell BE processor, the unit at 200 GFLOPS provides processing capacity that rivals that of 12 to 20 PowerPC processors or 45 Intel Pentium 4 processors. The enclosed unit is housed in a deployable ATR chassis about the size of a toaster.

large, powerful FPGAs with signal processing functionality. Next-generation UAVs are replacing the multiprocessing of big, power-hungry PowerPC-based boards, with more integrated boards with FPGAs. Where the original Global Hawk UAV, for example, embedded around 40 boards, today's system has replaced around 30 of those boards with just a handful of FPGA-based cards.

Targeting mainly networked land-mobile vehicles, Mercury offers a product that exemplifies the notion of high-density computing. Called the PowerBlock 200 (Figure 3), the system was Mercury's first rugged device designed with the Cell BE processor. The PowerBlock 200 processing appliance is designed to deliver the raw compute power needed to propel the vision of network-centric warfare from the research laboratory into the field. At 200 GFLOPS, the processing capacity of the PowerBlock 200 rivals that of 12 to 20 PowerPC processors or 45 Intel Pentium 4 processors. The unit is enclosed in a deployable ATR chassis about the size of a toaster.

The PowerBlock 200 uses a 1/2 ATR Long Tall chassis designed for military applications in the harshest environments on land, sea and in the air. It con-

tains a single Cell BE processor and has Gigabit Ethernet, Fibre Channel, RS-232 and GPIO front panel interfaces. Other I/O options are available via open-standard mezzanine card expansion sites. The entire chassis will consume less than 400W and support a self-contained cooling infrastructure that will conduct heat to the chassis walls. ■■

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Tundra Semiconductor Satisfies Parallel And Serial VME Design Requirements

After 25 years VME is still flourishing.

In 1999 Tundra introduced the industry leading Universe™ a PCI-to-VME bridge chip. It quickly became the de facto standard for VME64 backplane. Today, VME system designers are considering a number of different interconnect choices to enhance the performance of the VME chassis. They can choose to increase the VME bus speed with new VME protocols such as 2eVME (also known as VME160) or 2eSST (also known as VME320), or adopt one of the new serial based interconnect standards such as RapidIO®.

In 2003 the introduction of the Tundra Tsi148™ PCI-X-to-VME Bridge boosted VMEbus bandwidth by eight times with its 2eSST interface. 2eSST is compliant with the ANSI/VITA 1.5-2003 standard and designs built to this specification will support rates up to 320 Mbytes/second in a 21 card backplane implementation. The Tsi148 is also fully backwards compatible with older VME standards.

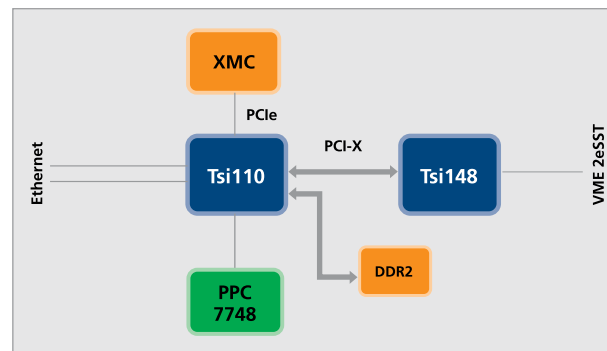
For those looking for even more of a performance boost RapidIO has emerged as an ideal choice for many VME systems. The addition of high speed serial interconnect using Serial RapidIO Switches to the VME chassis greatly increases its performance potential while offering backwards compatibility needed in these plug and play systems.

Tomorrow's systems that employ high-speed serial connections offer the ability to design a truly distributed computing system. Serial RapidIO-based connections with low latency and high bandwidth means multiple processors and memory can be connected across a backplane in a very effective manner. This has many system benefits; scalability through card upgrades, power management through distribution on the heat producers, and system optimization through the use of task specific processors.

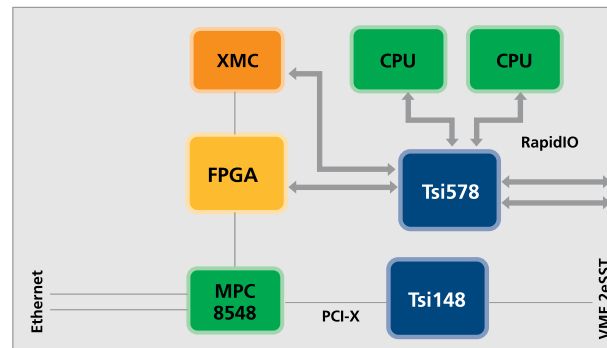
Serial interconnect is specified in both VITA 41 (VXS) and VITA 46 (VPX) VME systems, but multiple choices have slowed adoption rates as companies wait for a clear winner to emerge. These serial fabric choices – ranging from Ethernet, InfiniBand, PCI Express®, HyperTransport™ and RapidIO – narrow significantly when key criteria are applied. Low latency, high bandwidth, and error management are required by VME customers to build distributed

computing platforms with the reliability and scalability expected. For these requirements, RapidIO has been a winning solution for VME systems. Tundra's family of Serial RapidIO Switches along with RapidIO-enabled, processors, DSPs and FPGAs have made the selection of this standard for VME an ideal option.

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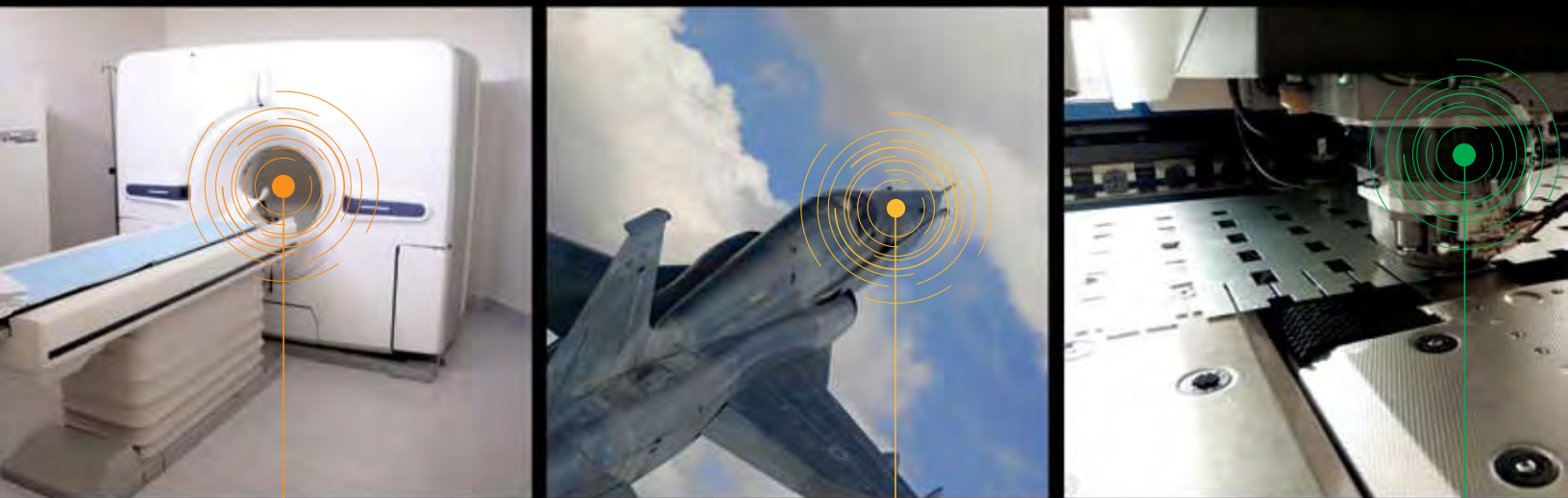


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Special Feature

Nano and High-Density Computing

High-Density Computing Fuels Fusion of Embedded Visual Information

Small, lightweight, integrated visual computing systems are enabling military solutions that convert raw data and process sensor input to create true information fusion.

Mark Snyder, Senior Principal Engineer
Quantum3D

Today's battlefield is dominated by visual information. Much of the embedded computing power on today's battlefield is dedicated to processing video information—capturing it, transmitting it and displaying it within C4ISR systems. Unmanned vehicles add the capability to generate yet more visual information. Communications links and C4ISR applications are overwhelmed. Looking toward the future, two trends will dominate visual computing—sensor and video processing embedded with sensors, and improved highly embedded, low-power video/graphical processing at the point of the spear.

Both technologies are required to streamline the future network-centric battlefield. The goal of the first is to embed the process of gaining information from raw data into sensor processing systems, reducing the requirement for high-bandwidth communications to move raw data. At the other end of the spectrum, the second technology trend seeks to enable the consumer of sensor-derived information with the embedded visual computing power required to create information fusion, as opposed to merely display raw data.

This fusion must be embedded in small, lightweight, integrated visual com-



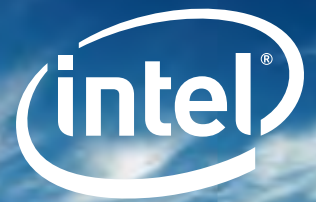
Figure 1

A Stryker soldier uses the FBCB2 system in the field. The FBCB2 allows units to communicate through a hardware-software program that provides an almost real-time picture of the battlefield, providing troops with greater situational awareness.

puting systems to be effective—the large footprint, stovepiped computing architectures used today will not suffice. It's important to understand the technology developments driving these trends and discuss what the embedded computer industry needs to provide to make this vision a reality.

The State of Network-Centric Warfare

Information dominates on the battlefield of today. Much of this information is visual in nature. Visual information ranges from powerful 3D digital moving maps to raw video gained from sen-



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processor platforms of all types (Figure 1). The information architecture of the network-centric battlefield, such as that envisioned for Future Combat Systems (FCS), is designed to allow all sorts of visual information to be collected, stored and offered in a publish-subscribe manner to multiple levels of command.

A “Common Operating Picture” (COP) unifies the battlespace picture in

a manner that visually depicts units, enemy intelligence information, operational plans, map data, sensor data and myriad other information. Visual sensors—including the human eye—feed into the decision-making process at many levels in the creation of the COP, and timely information is critical. Visual sensor information is used to locate suspected enemies, to assess effectiveness of attacks,

to monitor areas of interest, and is sometimes used in real time during an attack, such as the much-discussed “live” video images used to direct UAV-based missile attacks in real time.

This pipeline of on-demand visual information, available in its raw form, is only a part of the picture. The goal of many new sensor platforms, such as small unmanned vehicles, is primarily to provide raw visual information in near real time via stovepiped dedicated links. The data from these platforms may be recorded, and can potentially be resent over other links for use by other systems. As such visual platforms multiply and become available to more levels of command, the communications pipelines available to move the information are not adequate to the task. A major challenge of new information architectures, such as FCS, is to enable more bandwidth.

Data timeliness is another major challenge for visual systems on today’s battlefield. A digital mapping system, for instance, relies on geospatial information in many forms, which is produced and correlated by many different orga-

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Figure 2

Shown here is a Quantum3D Liberty VPX GPU Algorithm Accelerator (top) employed to extract target data from real-time, high-definition sensor returns (bottom).

nizations. Most geospatial information systems employed on the battlefield prestore this visual information on the computer system used to view the data, resulting in information becoming out of date over time.

Enabling Algorithm-Based Sensor Processing

Several trends in embedded visual computing provide the means to address visual information overload on the battlefield. One important trend is embedding visual computing resources with sensor platforms, with an eye toward automated extraction of interesting information from sensors. Embedded visual computing engines, such as arrays of graphical processing units (GPUs), can be used to analyze large amounts of sensor data and extract information from it.

By embedding such algorithms as pattern recognition, computer vision, or 3D reconstruction techniques in these algorithm accelerators, raw information can be turned into metadata. For instance, a LIDAR sensor can be used to generate 3D building forms automatically from raw data, and the existence of the 3D building and its geometry can be described and transmitted, rather than the raw sensor image itself.

The technology to build such algorithm accelerators and to embed them closely tracks technology used in advanced video games. Video game processors use advanced GPUs, which are high-performance pixel processors that are primarily used to create visual representations of scenes from data describing the scenes, including geometric data, lighting information, material properties and embedded programs called shaders that describe mathematical transformations used to render realistic scenes. A GPU-based algorithm accelerator can be thought of in some ways as performing GPU visual representation processing in reverse—taking observed properties of a visual or sensor representation and working backward to the information that the observed data implies.

These GPU algorithm accelerator architectures are basically high-per-

formance floating-point parallel pixel processing pipelines. There is much ongoing work in designing embedded computing platforms capable of being used as parallel algorithm accelerators. Embedded GPUs are being deployed in these new architectures to build the required capability. Such embedded sensor processing will become more prominent as the nexus of net-centric

warfare shifts toward information fusion. At the other end of the information fusion pipeline is the consumer of the information, and here also embedded visual computing is evolving to meet the needs. Figure 2 shows a Quantum3D Liberty VPX GPU Algorithm Accelerator employed to extract target data from real-time, high-definition sensor returns.

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Decisive Data at the Right Place and Time

As data moves from its raw form into usable, geo-registered metadata, the systems used to view the data must also evolve. The typical stovepiped information architectures with dedicated visual computing capabilities geared toward near real-time presentation of raw sensor data must give way toward a new archi-

ture, stressing information fusion. The ability to fuse data from many sources, stored data, raw sensor data, metadata gleaned from sensors and operational planning information must be provided. And, in the urban operational climate dictated by the realities of the war on terror, the information must be provided in new ways that enable the soldier to understand 3D environments and to exploit

the information in natural manner.

The computing platforms employed to present this information must also be smaller, lighter, cheaper and consume less power, for the typical consumer of the information may be a dismounted infantry. The challenge of fusing data is enormous, but, here again, embedded visual computing is an important component of the solution.

The same concept of the GPU is a major element in the embedded end-user computer on the information battlefield. The process of constructing a visual representation of all the information must be data-driven, and must efficiently employ the limited computing resources to present the needed display. As in the sensor algorithm accelerator, high-performance parallel floating-point processing is required, this time to rectify, fuse and layer the required visual information, in 2D and 3D views.

Ingesting and Representing Visual Data

GPUs provide a natural means to ingest visual information and to rectify it through stretching, rotation, or draping it onto a terrain representation. Live sensor data can be similarly rectified and placed in context on the information fusion display. Finally, symbols representing metadata, known data, or operational plans can be added into the visual representation to create an information fusion display. The processing to create the information fusion display can be hosted on even a small, lightweight computing system if it employs GPU technology. In this regard, systems based on technology used for mobile gaming devices or other small, low-power computers are ideal. Figure 3 shows a Quantum3D Thermite TL employed to generate a 3D information fusion display.

Network-Centric Warfare—Situational Awareness—whatever you call it, information is the key to the battlefield. Many computing systems are deployed on the battlefield solely for the purpose of enabling the warfighter to gain, distribute and employ information. As the means to collect information grows exponentially, embedded visual computing technology

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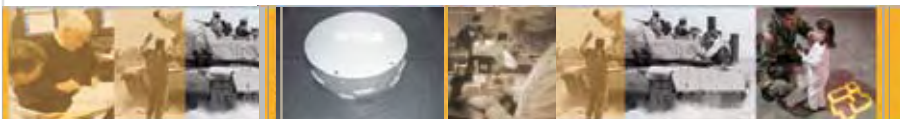
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becomes a more and more important part of the solution.

Exploiting the powerful floating-point capabilities found in GPUs to both analyze and extract information from raw data and to construct an information fusion view from data is a key part of the technological solution to this challenging problem. The embedded computer industry can leverage advances made in entertainment technology to make the job easier, but in the end, a thorough understanding of visual computing architectures and the information they process is necessary. Merely adding GPU capabilities as an afterthought to existing computers will not be enough. ■■

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Figure 3

Shown here is a Quantum3D Thermite TL (top) employed to generate a 3D information fusion display (bottom).

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Grant Hulse, Vice President of Marketing
Simtek

It's long been a given that military system designers are dependent on the shifts and directions of the general commercial computing and consumer markets in terms of available memory technology choices. Except for the most niche military and aerospace applications, engineers have been forced to go with something close to the DRAM, SRAM or flash architectures that dominate the PC or consumer device markets. While those architectures haven't lined up exactly with military system requirements, the recent emergence of nvSRAM at reasonable densities looks to be a favorable trend for defense system designers.

Common to virtually all electronic systems, military systems ranging from UAVs and UGVs to portable systems require non-volatile memory for program storage, configuration data and changes that are stored during unexpected power loss. The dilemma has been that non-volatility has traditionally been incom-

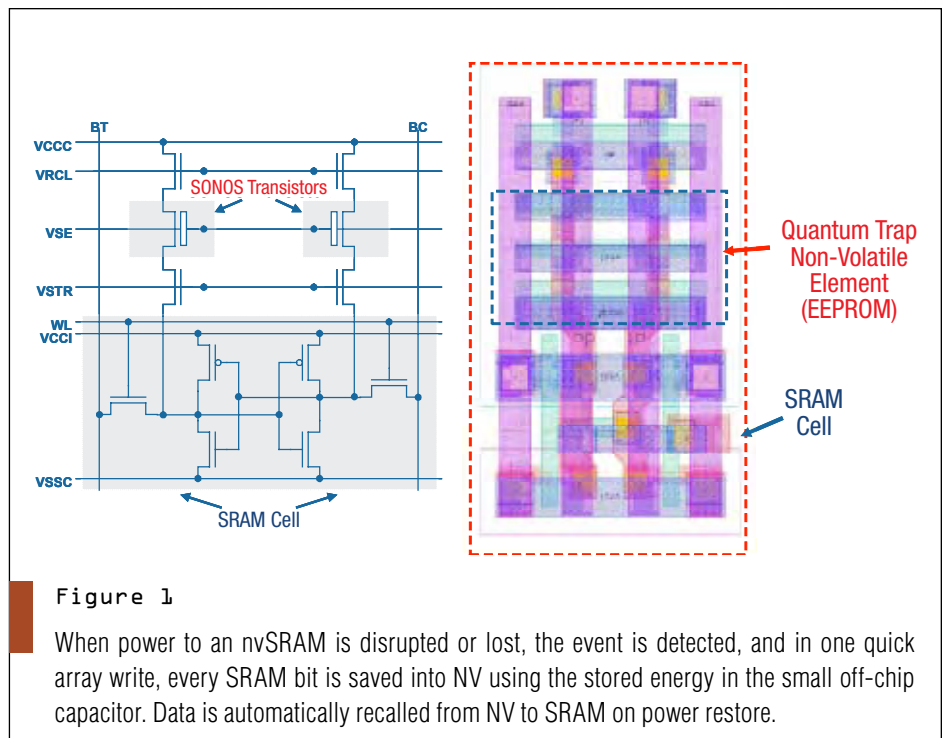


Figure 1

When power to an nvSRAM is disrupted or lost, the event is detected, and in one quick array write, every SRAM bit is saved into NV using the stored energy in the small off-chip capacitor. Data is automatically recalled from NV to SRAM on power restore.

patible with high performance, efficiency and functional integration. As a result, selecting a non-volatile memory solution has required a trade-off that balances speed, power, density, performance, board space, reliability and the price of available devices. Optimizing the trade-off, or finding an alternative, is crucial in the growing number of handheld military

devices, embedded computer systems, intelligent peripherals and autonomous military systems.

Traditional memory system architectures combine non-volatile memory—such as EEPROM or flash—with volatile memory (SRAM or DRAM). Such an approach compromises performance and reliability to gain function-

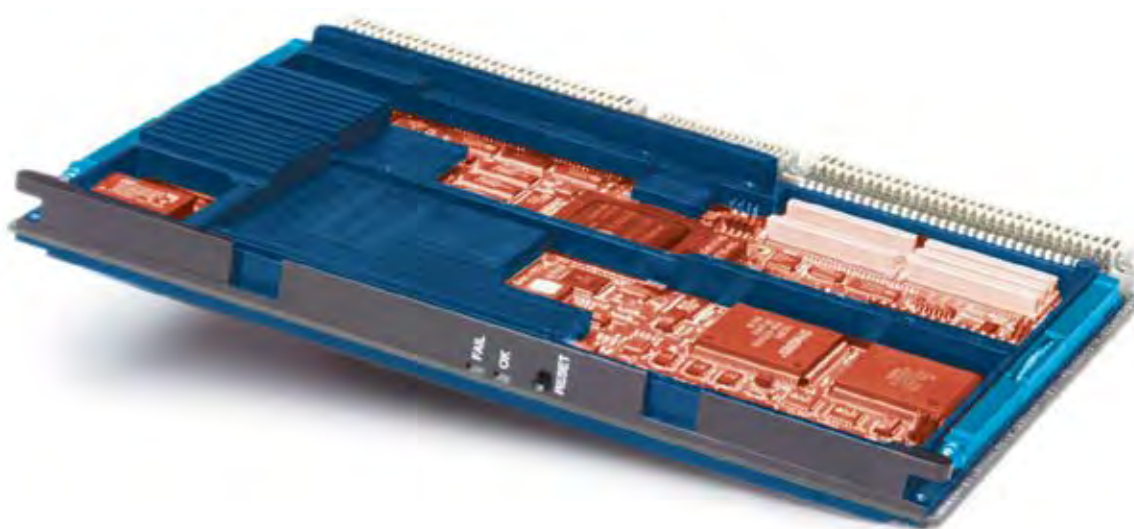


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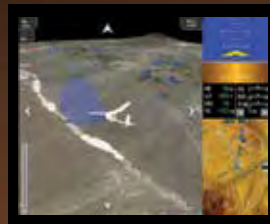


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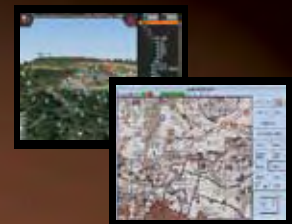
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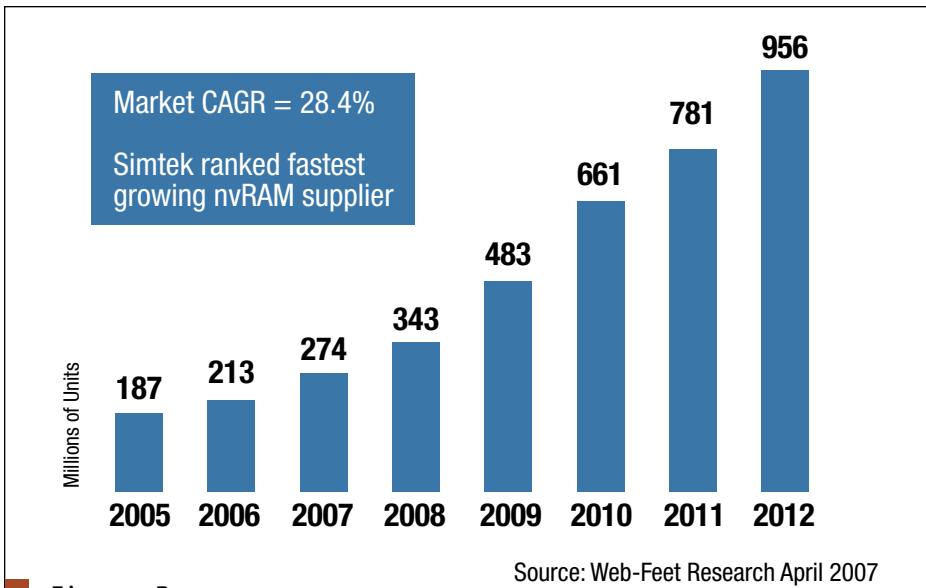


Figure 2

Web-Foot Research is forecasting a healthy 28 percent compound annual growth rate for nvSRAM through 2013. In addition to the traditional markets, it's expected that another "parallel universe" of opportunities for nvSRAM will begin to emerge in 2008 and 2009.

ality. Another approach combines the features of a fast static RAM with a non-volatile EEPROM into a single device: the nv (non-volatile) SRAM.

SONOS-Based nvSRAM Products

As the enabling process technology behind nvSRAMs scales to 130 nm and below, designers now have 40 percent better access times, four to eight times higher densities and improved overall system performance with which to solve previously difficult non-volatile memory design challenges. Meanwhile, as nvSRAMs based on silicon oxide nitride oxide silicon (SONOS) process technology have evolved, including devices from Simtek, they are able to provide densities of up to 16 Mbits in stacked-die configurations, and fast access speeds down to 15 ns.

This new generation of nvSRAMs gives military system designers new latitude to optimize performance, reliability, space constraints, density and cost-effectiveness. And, since the nvSRAM replaces the multi-chip combination of non-volatile memory and SRAM used in a majority of applications, it allows systems to be designed or upgraded with a single device and minimal effort.

Against this backdrop, the latest generation of nvSRAM devices is now surpassing battery-backed SRAM, parallel FRAM, MRAM and EEPROM technologies in a wide variety of legacy applications. Table 1 compares the trade-offs between the various semiconductor memory technologies.

In system operation, the nvSRAM ICs behave exactly as standard fast SRAM and can be easily interfaced to existing microprocessors and microcontrollers. When IC power is disrupted or lost, the event is detected, and in one quick array write, every SRAM bit is saved into a corresponding NV bit using the stored energy in the small off-chip capacitor (Figure 1). Data is automatically recalled from NV to SRAM on power restore.

Long Endurance Cycles

As a result, the SONOS transistors are written to only once during each power cycle over the lifetime of the nvSRAM architecture, while still allowing infinite read/writes and access times down to 15 ns, because it uses only the SRAM portion of the NV cell during power on. Since the SONOS portion of the NV cell is only written to during a power inter-

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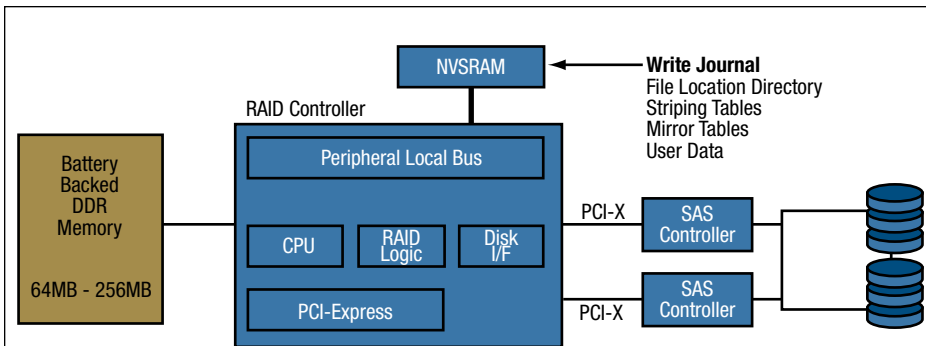


Figure 3

In RAID storage systems nvSRAM maintains the “write journal” records on data block placement across the array of disk drives. On power interrupt, or a failing disk, the data can be quickly rebuilt from the nvSRAM content.

ruption, the nvSRAM cell does not exhibit the typical endurance (wear out) issues as other non-volatile technologies. With as little as 200,000 cycles of endurance, the NV cell can withstand more than 50 power interruptions per day over the typical 10-year lifetime of a semiconductor device.

Many advanced military embedded computer systems, including DSP-based and RISC-based subsystems, require fast access to read-only or read-mostly memory. A typical system solution is to download the contents of low-performance non-volatile memory—ROM, EPROM or EEPROM—into high-performance SRAM devices and access the SRAM directly from the processor. For these systems, the nvSRAM provides the non-volatility of EEPROM and the high performance of SRAM in one component. Since the program held in the nvSRAM can be directly altered by the processor, portions can be designated to accommodate feature variants and code patches.

DSP system architectures are particularly demanding on memory I/O, busing and memory timing. In addition to program storage, DSPs require storage of coefficient data. This data is typically stored in read-only memory and downloaded to SRAM for execution. Among the drawbacks to this approach is increased busing complexity, which increases parasitic capacitance and control logic on the bus, making it difficult to achieve high performance.

With 15 ns read/write access time and 4 Mbits to 16 Mbits of storage, the nvSRAM offers high performance and ample storage space for DSP algorithms and coefficients. Single-chip DSPs, such as Texas Instruments’ DaVinci family and Analog Devices’ TigerSHARC, can be used with the nvSRAM to produce a complete two-chip DSP system, which is particularly useful in high-speed pocket modems, LAN adapters and embedded systems. In advanced DSP systems that use adaptive algorithms, the nvSRAM provides critical storage of data coefficients and parameters.

Low Life-Cycle Costs

For military system designers, the concept of cost is broader than considering single component prices. It also encompasses overall system life-cycle cost. This life-cycle cost includes such factors as the inventory cost of a single component vs. a multichip solution, board-manufacturing costs, reliability and maintenance issues.

Compared with other non-volatile system memory solutions, the nvSRAM reduces life-cycle costs. On a simple component level, nvSRAMs currently sell for about twice the price of battery-backed SRAM or SRAM-plus EEPROM solutions. However, the life-cycle cost of the nvSRAM is closer to parity with these options, because of lower inventory and manufacturing costs, higher reliability and lower system-design complexity.

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Special Feature

With non-volatility, 15 ns access time, and 4 Mbits to 16 Mbits of density, the current generation of nvSRAMs has features that make the devices a logical choice for many advanced system designs. This is particularly true in critical embedded systems, portable military instruments and remote applications. Future generations of nvSRAMs will follow the typical memory

learning curve and will soon approach the cost of alternate solutions at the component level.

Well Used, but Not Well Known

While not as well known as other memory technologies, nvSRAM's popularity has accelerated in recent years and will continue to grow into the future. For its part, nvSRAM vendor

Simtek continues to report that the nvSRAM has already been employed in over 1,000 different customer designs in a wide range of markets. The design-in rate has been accelerating in recent years. nvSRAM is used on board-level products from GE Fanuc Embedded Systems and Curtiss-Wright, as well as in military avionics and weapons systems by General Dynamics, Lockheed Martin, BAE Systems, Raytheon, Honeywell and Boeing.

Both the systems that use nvSRAMs and the application of nvSRAMs in those systems are increasing at a solid pace. Web-foot Research, which focuses its market research on the non-volatile memory space, is forecasting a healthy 28 percent CAGR for this market segment through 2013 (Figure 2). In addition to the traditional markets, it's expected that another "parallel universe" of opportunities will exploit nvSRAM and nvRAM products. These new opportunities will begin to emerge in 2008 and 2009.

RAID storage systems are a key component of many complex military systems—including radar and SIGINT systems and as back-end storage for military test and data acquisition systems. For Simtek, the largest revenue market in which nvSRAM has seen wide success is as part of the metadata storage system in RAID storage architectures where it maintains the "write journal" records on data block placement across the array of disk drives (Figure 3). On power interrupt, or a failing disk, the data can be quickly rebuilt from the nvSRAM content. Larger nvSRAMs can be used by the larger array storage systems as well, where the write journals become larger and more complex. The concept of having an nvSRAM memory serving a solid metadata storage block has exciting possibilities, as the industry continues to invest in ways to solve larger non-volatile problems and opportunities being created by flash technology's simultaneous increase in density, coupled with a decrease in durability.

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Parameter	Flash	EEPROM	SRAM	Battery-Backed SRAM	FRAM	Simtek nvSRAM
Non-volatile	X	X		X	X	X
Unlimited Endurance			X	X		X
Random Access			X	X	X	X
No Battery Needed	X	X	X		X	X
Fast Read and Write (25-45 ns)			X			X
Byte Programmable		X	X	X	X	X

Table 1

Compared here are the trade-offs between various semiconductor technologies.

Suited for Military Apps

Non-volatility is also important in a number of other military applications—such as missile-guidance systems, flight data recorders, smart munitions, satellites and navigation systems—to store configuration parameters and data. Space and weight constraints make a multi-chip EEPROM-plus-SRAM or a core memory solution impractical. In highly reliable military systems, ferro-magnetic core memory has been the only practical read/write non-volatile memory, despite its limited performance, low density and considerable cost.

Other solutions, such as batteries, are unacceptable in mission-critical defense systems and satellites. The nvSRAM provides a clear alternative for these systems. Simtek will use smaller cell sizes offered by 130 nm to bring many of the same advantages to the military markets that have also been offered to the automotive market, including superb performance at extreme hot and cold temperatures—something that several of the new non-volatile memory concepts cannot match.

Simtek's nvSRAM technology, with a combined SRAM and non-volatile monolithic approach, is an ideal fit for small, portable systems. Portable, handheld devices represent one of the most active and dynamic segments of military system design. The 130 nm nvSRAM technology, combined with simple interfaces (like SPI), will bring a new level of performance to these systems that always place a premium on

board space. In all portable systems, nvSRAM's non-volatile data storage (with zero current drain on the battery) is a strong selling feature, and the growth of SoC solutions with nvSRAM blocks will bring many new solutions to portable applications.

The nvSRAM Roadmap

As a 20-year champion of the nitride sandwich approach to non-volatility, Simtek has been granted a number of key patents for the application of nvSRAM technology. Over the next few years, SONOS process technology is expected to become much more pervasive in high-volume fabs as a non-volatile technology for memory blocks in System-on-a-Chip solutions, as well as for the Multi-level Cell and flash mirroring approaches with NAND flash ICs that are driving density in the large, diverse and demanding non-volatile memory markets. Volume increases in the NAND flash market will be driven by the ever growing quest for portability. SONOS flash will likely play a key role in enabling solid-state disks (SSDs) and driving down their price point, which will continue to allow SSDs to encroach on the multi-billion dollar hard disk drive market. ■■

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Tech Recon

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Simon Collins, Product Manager
GE Fanuc Embedded Systems

There are perhaps as many definitions of situational awareness as there are situations to be aware of. A consensus exists, though, that in its simplest form, situational awareness is about knowing what's happening so that an informed choice about future actions can be made. As such, it's not surprising that, as a term, it was first used by the military—specifically, U.S. Air Force aircrew in Korea and Vietnam. It's equally unsurprising that providing improved situational awareness to deployed forces is the focus of much investment on the part of the military.

What drives situational awareness is knowledge. That knowledge derives from information—and what drives that information is data. As Clint Eastwood



Figure 1

Today's military strives to gather data from almost any source including satellites, UAVs, traditional reconnaissance, databases, vehicles and individual troops. UAVs like the Global Hawk can remain on station capturing imagery, return and land. Ground-based operators monitor the UAV's status and can change navigation and sensor plans during flight as necessary. (U.S. Air Force photo/Master Sgt. Jason Tudor.)



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Bus													
AT Expansion Bus	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCI Universal Expansion Bus	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCI Bus Masters	4	4	4	4	4	4	4	4	4	4		4	
APIC (add'l PCI interrupts)	9	9	9	9	9	9	9	9	9	9			
CPU Max Clock Rate (MHz)	1400	1400	1400	1400	400	650	400	650	400	650	333	333	333
L2 Cache	2MB	2MB	2MB	2MB	256k	256k	256k	256k	256k	256k	16K	16k	16k
CPU and BIOS													
Intel SpeedStep Technology	✓	✓	✓	✓									
ACPI Power Mgmt	2.0	2.0	2.0	2.0	1.0	1.0	1.0	1.0	1.0	1.0			
Max Onboard DRAM (MB)	512	512	512	512	512	512	512	512	512	512	256	256	256
RTD Enhanced Flash BIOS	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Nonvolatile Configuration	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Quick Boot Option Installed	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
USB Boot	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			
Peripherals													
Watchdog Timer & RTC	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
IDE and Floppy Controllers	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
ATA/IDE Disk Socket, 32 DIP	1	1	1	1	1	1	1	1	1	1	1	1	1
Audio	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓			
Digital Video	LVDS	LVDS	LVDS	LVDS			TTL	TTL	LVDS	LVDS	TTL	TTL	
Analog Video	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	SVGA	
AT Keyboard/Utility Port	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PS/2 Mouse	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
USB Mouse/Keyboard	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
I/O													
RS-232/422/485 Ports	2	1	2	1	2	2	2	2	2	2	2	2	2
USB 2.0 Ports	2	4	2	4									
USB Ports					2	2	2	2	2	2	2	2	2
10/100Base-T Ethernet	1		1		1	1	1	1	1	1	1	1	1
ECP Parallel Port	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
aDIO (Advanced Digital I/O)	18	18	18	18	18	18	18	18	18	18	18	18	18
multiPort (aDIO, ECP, FDC)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SW													
ROM-DOS Installed	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
DOS, Windows, Linux	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

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AT Expansion Bus	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCI Expansion Bus Master	✓	✓				✓							✓	✓
McBSP Serial Ports	✓	✓				✓								
Analog Input														
Single-Ended Inputs	16	16	16	16	16	16								
Differential Inputs	8	8		8	8	8								
Max Throughput (kHz)	1250	1250	40	500	100	1250								
Max Resolution (bits)	12	12	12	12	16	12								
Input Ranges/Gains	3/7	3/7	3/1	3/4	1/4	3/6								
Autonomous SmartCal	✓	✓												
Data Marker Inputs	3	3		3		3								
Conversions														
Channel-Gain Table	8k	8k		8k	8k	8k								
Scan/Burst/Multi-Burst	✓	✓		✓	✓	✓								
A/D FIFO Buffer	8k	8k		8k	8k	8k								
Sample Counter	✓	✓		✓	✓	✓								
DMA or PCI Bus Master	✓	✓		✓	✓	✓	✓							✓
SyncBus	✓	✓		✓	✓	✓								
Digital I/O														
Total Digital I/O	16	16	16	16	16	16	16	48	18/9	32	64	32	48	48
Bit Programmable I/O	8	8		8	8	8	8	24	6/0				48	✓†
Advanced Interrupts	2	2		2	2	2	2	2					2	
Input FIFO Buffer	8k	8k		8k	8k	8k							4M	8M
Opto-Isolated Inputs										16	48	16		
Opto-Isolated Outputs										16	16			
User Timer/Counters	3	3	3	2	3	3	3	3	3				10	6
External Trigger	✓	✓		✓	✓	✓	✓	✓					✓	
Incr. Encoder/PWM									3/9					✓†
Relay Outputs												16		
Analog Out														
Analog Outputs	2	2		2	2	2	4							
Max Throughput (kHz)	200	200		200	100	200	200							
Resolution (bits)	12	12		12	16	12	12							
Output Ranges	4	4		3	1	4	4							
D/A FIFO Buffer	8k	8k				8k	8k							

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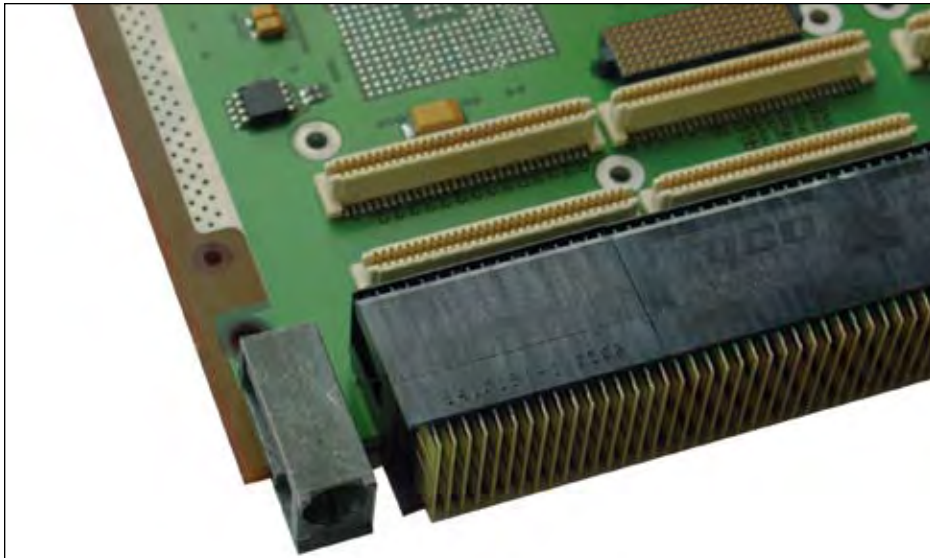


Figure 2

VPX offers a significant increase in I/O bandwidth derived from its implementation of the Tyco MultiGig RT2 connector. The connector is rated for signals up to 6.25 Gbits/s—around six times the capacity of the VME connector.

Four Computing Challenges

Collecting that data is a significant computing challenge. That said, it is but one of four computing challenges in situational awareness applications. Only a fraction of the data collected is valuable at any one point in time: delivering to the user huge amounts of raw, unanalyzed data will serve only to overwhelm and confuse. Situational awareness requires that the information presented be easy to assimilate and easy to understand—complex data must be easy to make sense of “at a glance”—if it is to form the basis of rapid action. The second computing challenge, therefore, is to winnow out the irrelevant data. Paradoxically, as significant an amount of computing power is deployed in discarding data as was expended in acquiring it in the first place.

For the information to become knowledge, it must, however, be complete. Information about the location of enemy vehicles, for example, is incomplete without information about the capabilities of those vehicles, the intervening terrain, or the position of friendly troops. Information about a target is inadequate if nighttime conditions preclude a detailed view of it. The

famously pointed out in *For A Few Dollars More*, “a man’s life in these parts can depend on the merest scrap of information.” He might have been talking about the military’s requirement for superior situational awareness.

The military has never been positioned to gather more data than it can

today. It can be gathered from almost any source: satellite, unmanned aerial vehicle (UAV) (Figure 1), traditional reconnaissance, databases, vehicles—even individual troops. It can come from cameras, sensors, the network. It can take an enormous variety of forms—video, graphics, infrared, sonar, radar, lidar (ladar).

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third computing challenge is to fuse together different sources of data and to present it as meaningful and actionable information. And, finally, the fourth computing challenge is the requirement to take the gathered, processed and fused information and to display it on-screen in close to real time. Information that is only a second out of date may be valueless—and possibly even disastrous—information.

Situational awareness is, by definition, an application that will, as a result of complex and demanding processing, output sophisticated graphics—whether as video, still images, symbols, icons or animations. From data acquisition to image output, it is highly computationally intensive and requires a computing architecture that offers the requisite bandwidth and raw processor power. Moreover, the optimum computing architecture will provide a natural platform for graphics-oriented applications because it will provide the potential for seamless integration with state-of-the-art graphics hardware. Increasingly, it seems that VPX is that architecture.

VPX Delivers the Goods

First and foremost, the VPX architecture is designed specifically to leverage the high performance that is inherent in serial switched fabrics such as PCI Express, Serial RapidIO, Gigabit Ethernet and InfiniBand, and their capacity to support the very high data transfer speeds required in networking, data storage (Serial SATA) and digital video (such as DVI, LVDS). Applications such as situational awareness require significant backplane streaming I/O, connectivity and bandwidth: VPX provides not only substantially more I/O pins, but it also enables bandwidths of up to 30 Gbytes/s—enabling more data from more sources to be captured than is possible with the more limited pin count of VME.

This significantly increased I/O derives from VPX's implementation of the Tyco MultiGig RT2 connector (Figure 2), which is rated for signals up to 6.25 Gbits/s

—around six times the capacity of the VME connector. Historically, connectors have incorporated pins arranged such that the vertical and horizontal pitch positions of the contacts are symmetric. It's an approach that works well for single-ended signals. However, the differential signals that characterize switched fabrics operate better over pairs of pins that are

close to each other, but that are as distant as possible from other pairs. Add to this the increased requirement for good grounding that arises as a result of much faster signaling speeds, and the need for a new connector technology becomes apparent. A 6U VPX board features six 16-column 7-row RT2 connectors and one 8-column 7-row RT2 connector, while a

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Figure 3

The VPX-based GE Fanuc Embedded Systems MAGIC1 Rugged Display Computer provides a 16-lane PCI Express interconnect between an Intel T2500 Core Duo CPU running at 2.0 GHz and an NVIDIA G73 GPU in order to deliver optimum throughput and performance.

3U board features two 16-column 7-row RT2 connectors and one 8-column 7-row RT2 connector.

Another, and not inconsiderable, benefit of the VPX architecture is that switched serial interconnects provide the foundation for highly robust, fault-tolerant architectures that can continue to operate in the event of the failure of an individual board. This contrasts with the parallel bus architecture of VME (or CompactPCI) in which failure of any single board will cause a total system failure. Given the mission-critical nature of situational awareness applications, this element of high reliability assumes great significance.

Support for Powerful CPUs

VPX also provides for the support of powerful processors, enabling both the processing required to turn the mass of data into a much smaller amount of information, and also to fuse that data together in order for it to represent knowledge. Where the VME specification allowed for no more than 30 watts of power dissipation per slot, VPX allows for significantly more: 115 watts at 5 volts, and up to 768 watts at 48 volts.

It does this through its use of dedicated power connectors in P0—as opposed to via signal pins in P1 and P2 as is the case with VME and, for that matter, CompactPCI. The implication is that VPX can accommodate the power dissipation of leading-edge processor silicon. For example, Intel's Core 2 Duo/Merom processor, designed specifically for low-power environments such as mobile computing, still dissipates 35W, and its 45-nm Montevina successor will allegedly dissipate 29W. Meanwhile, Freescale's 8641D dual core processor dissipates somewhat less, with around 19W at comparable processing speed. But more importantly, VPX accommodates the increasing functional density of today's highly integrated single board computers.

The combination of high-bandwidth I/O and powerful processing—which includes not only traditional general-purpose processing, but also



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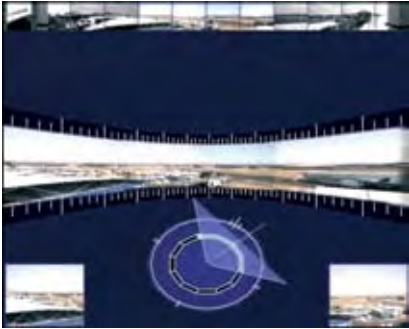


Figure 4

Shown here is the display from a 12-camera distributed aperture sensor system. At the top are the 12 individual video images. In the center is the viewed segment of the stitched panorama, in this view showing the combined image of two sensors. The relative position of the view is displayed by the lower central graphic while “views of interest” from two of the sensors are displayed in the bottom corners of the picture.

multiprocessing, digital signal processing and FPGA-based processing—that characterize the VPX architecture make a formidable contribution to its suitability as the basis for a compute-intensive, data-intensive application like situational awareness. It provides for the acquisition of substantial amounts of input data from a variety of sources, and for processing that data. In fact, it goes beyond the requirements of today’s applications and provides the possibility of enhancing them.

Take digital mapping, for example—a key element of situational awareness applications. Many of today’s digital mapping applications feature 2D, rather than 3D, presentation. One of the factors contributing to this is that the data points from which the terrain data is derived are sufficiently far apart that, when rendered in 3D, the resulting image appears as a number of jagged edges, rather than the smooth contours that are the reality. Sophisticated software exists that would al-

low this image to be smoothed in multiple directions—but the processing overhead invoked is considerable. The support provided by VPX for greater bandwidth and more powerful processing would allow this processing to take place—thus improving the quality of the map presented on screen.

On-Screen Data Challenge

Historically it’s been the presentation of on-screen data that has most challenged military applications. Here again, though, VPX brings important benefits when PCI Express is implemented as the primary serial switched fabric—as it is on the GE Fanuc Embedded Systems range of VPX single board computers.

The attraction of PCI Express is that it is the native interconnect technology for desktop computing, and thus provides simple and cost-effective access to the enormous number of devices and technologies designed for the PC environment. This is especially true of PC gaming technology, as characterized by products from companies such as NVIDIA—technology that promises to revolutionize not only situational awareness applications, but also other military applications such as simulation and embedded training.

The VPX-based GE Fanuc Embedded Systems MAGIC1 Rugged Display Computer (Figure 3), for example, provides a 16-lane PCI Express interconnect between an Intel T2500 Core Duo CPU running at 2.0 GHz and an NVIDIA G73 GPU in order to deliver optimum throughput and performance. It also features up to 64 Gbytes of SATA-connected storage, and a Gbit Ethernet interface. The SBC340 single board computer at the heart of the MAGIC1 is specifically designed to take maximum advantage of the silicon potential of both the Intel chipset and the NVIDIA GPU, the latter being the ideal platform for providing the real-time graphics processing—smoothing, fusing, overlaying and so on—required by the application.

Such a display processor might well find itself deployed in a fighting



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vehicle, where an element of the situational awareness requirement is to deliver to the crew a 360 degree view of the environment in which they find themselves (Figure 4). This view is generated by an array of distributed aperture video sensors (both TV and IR), which must operate in real time in order to be operationally effective. Previous processing architectures have not had the “bus power” to handle multiple, real-time video signals; VPX, with its associated PCI Express bus, now offers this capability.

Multiple Sensor Views

Like all elements of situational awareness, this multiple sensor view is of maximum value only when it has been “processed” in order to highlight items of interest to the overworked “operator.” In order to meet this requirement, Distributed Aperture Sensor (DAS) systems have both a detection and classification

element (data extraction) and an image stitching, aligning and formatting element (visualization). The former is a highly computationally intensive task for which the VPX CPU is ideally suited, while the latter can most effectively be accomplished in the VPX GPU.

The 3U VPX form-factor overcomes many of the inherent disadvantages of VME in its 3U guise, making it ideal for deployment in space-constrained, weight-constrained environments. The input from image sensors/cameras around the vehicle will be correlated and stitched together into a cohesive, panoramic whole. If necessary, infrared images will be overlaid, allowing detail to be discerned despite the lack of light or, for example, because of the presence of smoke or mist. Overlaid will be terrain and mapping data that, together with the acquired visual data, will provide a complete, fused view of any possible threats—before the hatch is opened.

There can be little doubt that the VME architecture will continue to be at the heart of demanding military embedded computing applications for many years to come. However, it looks likely that, for demanding graphics applications such as situational awareness, VPX brings with it a set of characteristics—substantial I/O bandwidth, ability to leverage leading-edge processor- and board-level silicon, native access to state-of-the-art graphics processing and inherent fault tolerance—that will see it become the architecture of choice. ■■

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Multicore Processing Feeds Military Imaging Needs

The high-end graphics/image processing needed in situational awareness applications depends on multicore processing and high-performance, low-power, small form-factor boards with a wide range of I/O.

Matt Stevenson, Principal Architect
WIN Enterprises

With the massive data sharing that will be made possible by the DoD's planned Global Information Grid (GIG), field and strategic commanders will be able to obtain real-time situational awareness data for tactical planning. The build-out of this grid, combined with advances in situational awareness technology, has driven a demand for server-class systems capable of high-end graphics and imaging processing and display.

Designers of military graphics and imaging subsystems need not only high-speed video, along with storage for the video data and for records purposes, but also high-speed data communication connections in order to share this field data with command centers or bases. Video streams coming in to the server from mobile devices used by individual warfighters on foot, in tanks or in other military vehicles must be stored, analyzed and/or sent out for further analysis to other locations.

Graphics/Imaging Design Challenges

For example, the soldier in charge of the server-class imaging system car-

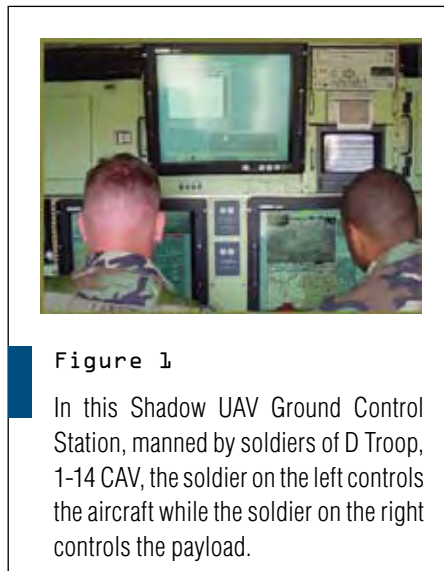


Figure 1

In this Shadow UAV Ground Control Station, manned by soldiers of D Troop, 1-14 CAV, the soldier on the left controls the aircraft while the soldier on the right controls the payload.

ried in a ground vehicle may not be an expert in the specific type of data analysis needed for tactical awareness in an urban warfare scenario, and must therefore send that data elsewhere to be analyzed. Consequently, the system must be capable of handling large amounts of incoming and outgoing data, as well as processing large amounts of data locally for real-time response.

Both high performance and a small, low-power form-factor are

highly desirable in the single board computers (SBCs) that serve as a design platform on which these server-class systems are based. So is enough bandwidth to enhance the processing of complex image data from multiple sources, such as UAVs (Figure 1) sending terrain overlay system data and live video, along with high-quality audio and a wide range of I/O choices to handle those multiple data streams. Since some data needs to be stored locally, large amounts of RAM and storage capacity are required.

To accomplish all of this, what's needed in an SBC design platform is multi-processing, along with the ability to handle large amounts of memory, and support for high-speed networking to send pertinent data out to other groups (Figure 2). In addition, an integrated storage controller, such as SAS, is desirable for high-density local storage arrays. In order to get all of this processing muscle, memory and I/O in a small space without consuming too much power, multicore processing combined

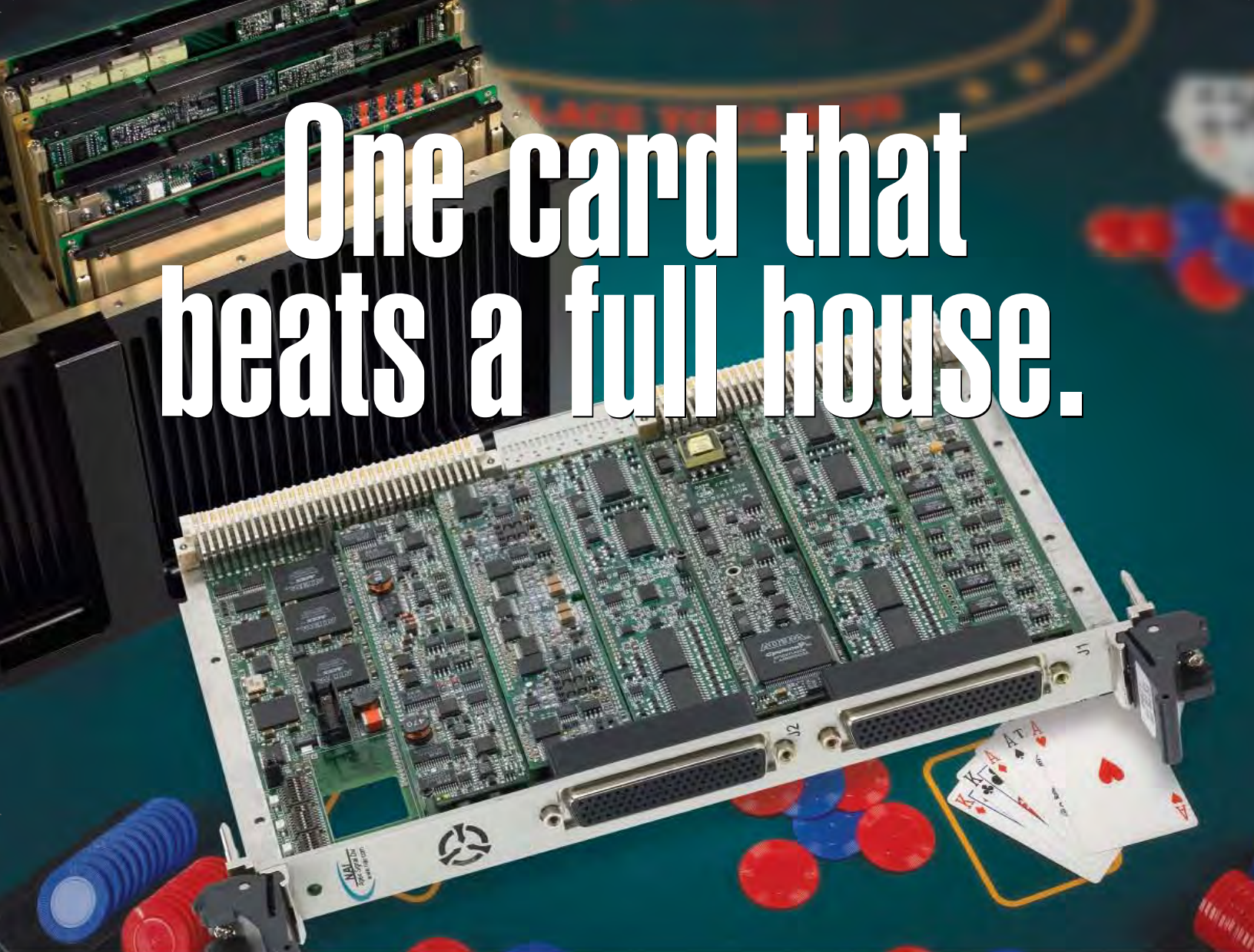


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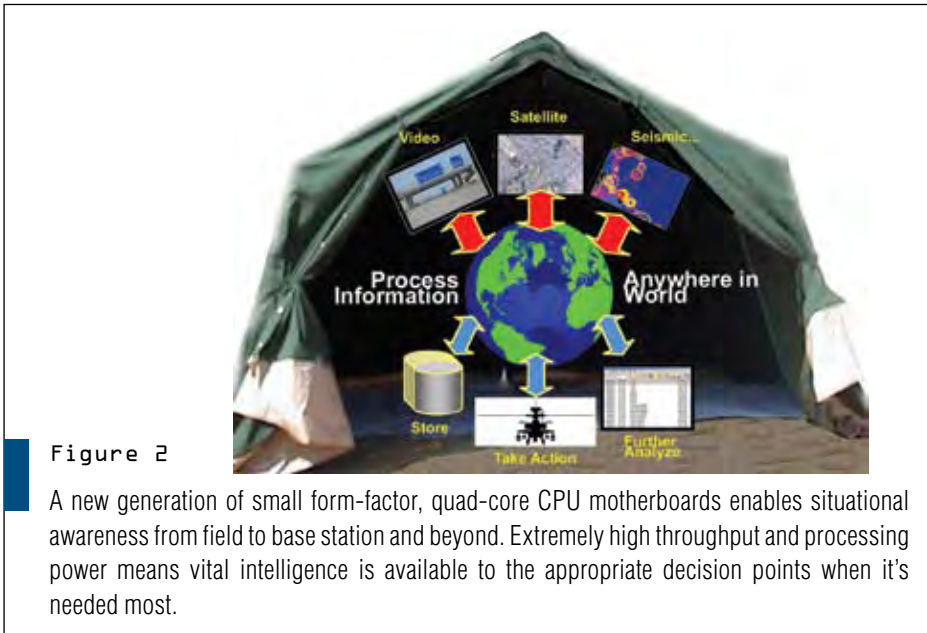


Figure 2

A new generation of small form-factor, quad-core CPU motherboards enables situational awareness from field to base station and beyond. Extremely high throughput and processing power means vital intelligence is available to the appropriate decision points when it's needed most.

with careful architecting of the SBC and the I/O control are required.

Quad-Core, Eight-Core Processing

Symmetric multi-processing (SMP) is already used for a number of multi-tasking applications in compute-dense military systems. The architecture is well suited for running multiple, concurrent tasks, such as processing different types of incoming data streams. Because of shared memory functions, combining SMP with multicore processing increases performance without consuming the large amounts of power of an equal number of separate processors. Since performance per watt is a key factor in military designs, multicore processing is being increasingly used to improve the speed and overall performance of many electronic defense systems, including SIGINT, radar, sonar and situational awareness.

Intel's 32-/64-bit Quad-Core Xeon 5300 (Clovertown) CPUs are the industry's first quad-core processors for standard, high-volume, two-processor (twin-socketed) server platforms. At 3 GHz per processor, their performance is up to 50% better than the company's Dual-Core Xeon 5100. In the low-voltage L5320 and L5310 versions, each core burns only 12.5 watts of power. The large 8 Mbyte

L2 cache for each quad-core processor enables very fast data transfers between processor cores.

The Intel 5300 series brings several benefits to high-end graphics and image processing. The high-speed, dual quad-core processors excel at the heavy number crunching and data processing that are necessary for processing the multi-threaded video, imaging and location information for situational awareness applications. Because of the dual quad-core processors' floating-point unit and the shared memory between each set of two execution cores, each execution core is faster than previous generations of high-performance single-core processors.

Eight Processing Threads

Shifting from dual-core to quad-core processors increases the number of threads available for multitasking and allows a server-class system to run more applications with a smaller footprint. Implementing a pair of quad-core processors in a board-level platform increases the number of threads to eight. An example along those lines is WIN Enterprises' MB-06063 (Figure 3). The MB-06063 implements dual, quad-core 5300s in a PICMG 1.3 SBC. This SBC is one of the first CPU boards for embedded OEMs that takes advantage of dual,

quad-core CPUs. Each processor has an independent, 1066/1333 MHz system bus. The twin-socketed board supports either Intel's Dual-Core 5100 processors or Quad-Core 5300 processors, and works exclusively with the low-power versions of these CPUs.

The Intel chipset provides increased graphic performance, reduced power consumption, platform reliability and system manageability. The South Bridge chip, the 6321ESB I/O Hub Controller, enables particularly feature-rich I/O, including PCI Express (PCIe) and PCI-X card edge connectors, multiple USB ports, and interfaces for AC97 audio and IDE hard drive storage. Additional I/O includes dual Gbit Ethernet, six SATA ports with RAID, a PATA port and serial interfaces.

PCI-X on the board enables connections to high-end storage and expansion of storage or high-end communications equipment, while 20 lanes of external PCI Express enable the use of commercially available plug-in cards such as dual graphics cards or high-bandwidth video capture cards. PCIe also allows connections to mass storage and high-speed networking devices. WIN Enterprises engineered this SBC, the MB-06063, so that even more I/O could be integrated in the small, PICMG 1.3 form-factor.

Additional internal lanes of PCIe have been utilized to integrate an ATI X300 Radeon Mobility graphics controller with 64 Mbytes of video RAM, a FireWire chip on a standard PCI bus and an eight-port, 3 Gbit/s LSI 1068 Serial Attached SCSI (SAS) controller.

Advanced Video Support

Most server-class machines either do not provide for video or only accommodate the lowest of low-end graphics cards. In this SBC, external DVI can be connected to the integrated ATI X300 graphics controller. Alternatively, graphics support is provided for VGA and LVDS, for integrated LCDs. Users can thus natively plug a display into the same box that houses the processor board, instead of being required to use a bulky external display with its own dedicated graphics display architecture.

An ATI X300 graphics card is a mid-

range card suitable for most video applications, except for those requiring large amounts of high-end 3D rendering. Since FireWire is the native interface in much of the video world, the integrated FireWire chip eliminates the need to configure a separate card for high-performance video, which is not normally the case in PICMG 1.3 form-factor devices.

The SBC provides up to 48 Gbytes of RAM in six FB-DIMM slots that reside on a plug-in daughter card. Although the Intel 5000P North Bridge chip allows the option of plugging in up to eight of these memory modules, other PICMG 1.3 form-factor implementations have to date only achieved a maximum of four.

Most Intel 5000P series-based PICMG 1.3 CPU cards consist of only a plain motherboard. With careful architecting, the MB-06063 dual, quad-core SFFB technology integrates plenty of memory, storage connectivity, native high-performance video capability, communications connectivity and high-bandwidth pro-

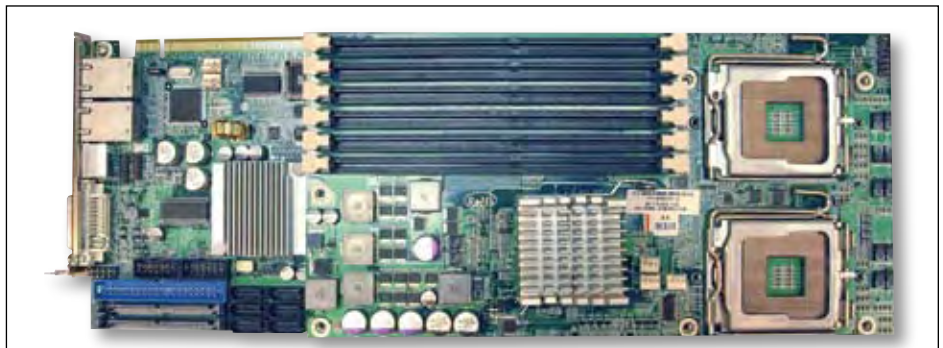


Figure 3

One of the first CPU boards for embedded OEMs to take advantage of quad-core CPUs, the WIN Enterprises MB-06063 PICMG 1.3 SBC, is based on Intel's dual Quad-Core 5300 Xeon CPUs. The I/O-rich board includes PCI-X, 20 external lanes of PCI Express, an integrated ATI X300 graphics controller with 64 Mbytes of video RAM, an integrated FireWire chip and an integrated eight-port, 3 Gbit/s LSI 1068 SAS controller.

cessing power to meet the needs of graphics and image processing for situational awareness applications. ■■

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PC Instrumentation Gear Eases SIGINT Analysis Chores

Fast fabrics like PCI Express and improved hard drive disk speeds are bringing RF stream-to-disk systems to bear on SIGINT analysis problems.

David Hall, RF and Communications Product Marketing Engineer
National Instruments

Signal intelligence (SIGINT) describes a broad range of applications—performed by the military and other government entities—ranging from communications jamming, packet sniffing and identification of interference or pirating signals. Such applications often require sophisticated and highly customized signal processing methods to characterize the power, frequency and phase of interference signals over long periods of time.

In many scenarios, the traditional approach to signal intelligence using bench-top vector signal analyzers and spectrum analyzers is insufficient because of the limited acquisition sizes of these instruments. However recent innovations in the PC industry such as the PCI Express bus and improved hard drive disk speeds enable PXI instruments to be used in RF stream-to-disk systems using off-the-shelf instrumentation (Figure 1). In fact, today's PXI-based RF stream-to-disk solutions enable the recording time-continuous RF bandwidth at frequencies up to 2.7 GHz. In a typical system, a 2 Terabyte RAID (redundant array of independent disks) system enables you to stream up to 20 MHz of RF bandwidth

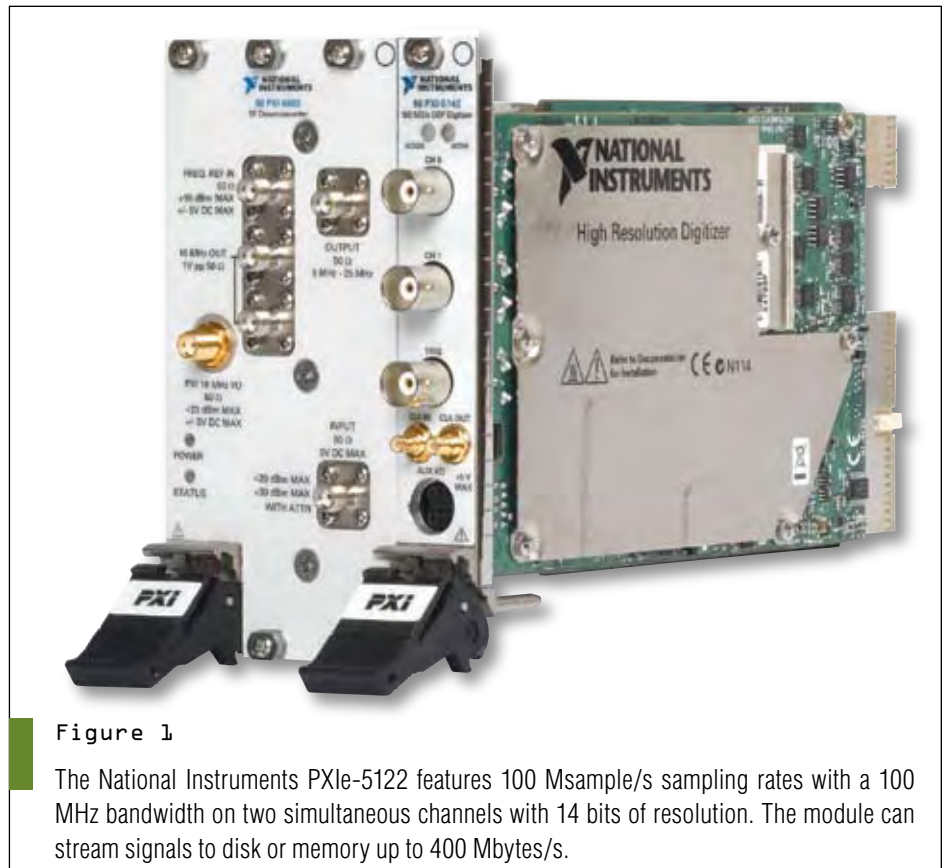


Figure 1

The National Instruments PXIe-5122 features 100 Msample/s sampling rates with a 100 MHz bandwidth on two simultaneous channels with 14 bits of resolution. The module can stream signals to disk or memory up to 400 Mbytes/s.

to disk for five hours or more.

There are two main types of interference signals each requiring a differ-

ent analysis technique typically used to identify them. These two types of interference signals are “jamming” sig-

nals, which obstruct communication channels, and pirating signals, which attempt to use existing communications infrastructure in an unauthorized manner. While both are considered interference signals, the motivation behind each type of signal, as well as the analysis techniques used to characterize them, are different.

Strategies for Analyzing Jamming Signals

Particularly in military scenarios, it is often necessary to identify interference from systems attempting to obstruct a communication channel. Frequently called jamming signals, this type of interference signal is able to jam a communication signal by producing unwanted power within the band of interest. Moreover, there are various types of signals that are commonly used as jamming signals. Common types of jamming signals include: single tones, random white noise, pulsed signals, frequency hopping signals and modulated “fake” communications signals.

Each of these produces trade-offs between effectiveness, power requirements, ease of generation and difficulty of detection. For example, generation of a single carrier in an existing communication channel is relatively simple. However, a single carrier is often ineffective and is easy to detect. On the other hand, generation of broadband white noise can be extremely effective at obstructing a communications link. Although this method results in significant power requirements and is easy to detect if the signal is not periodic.

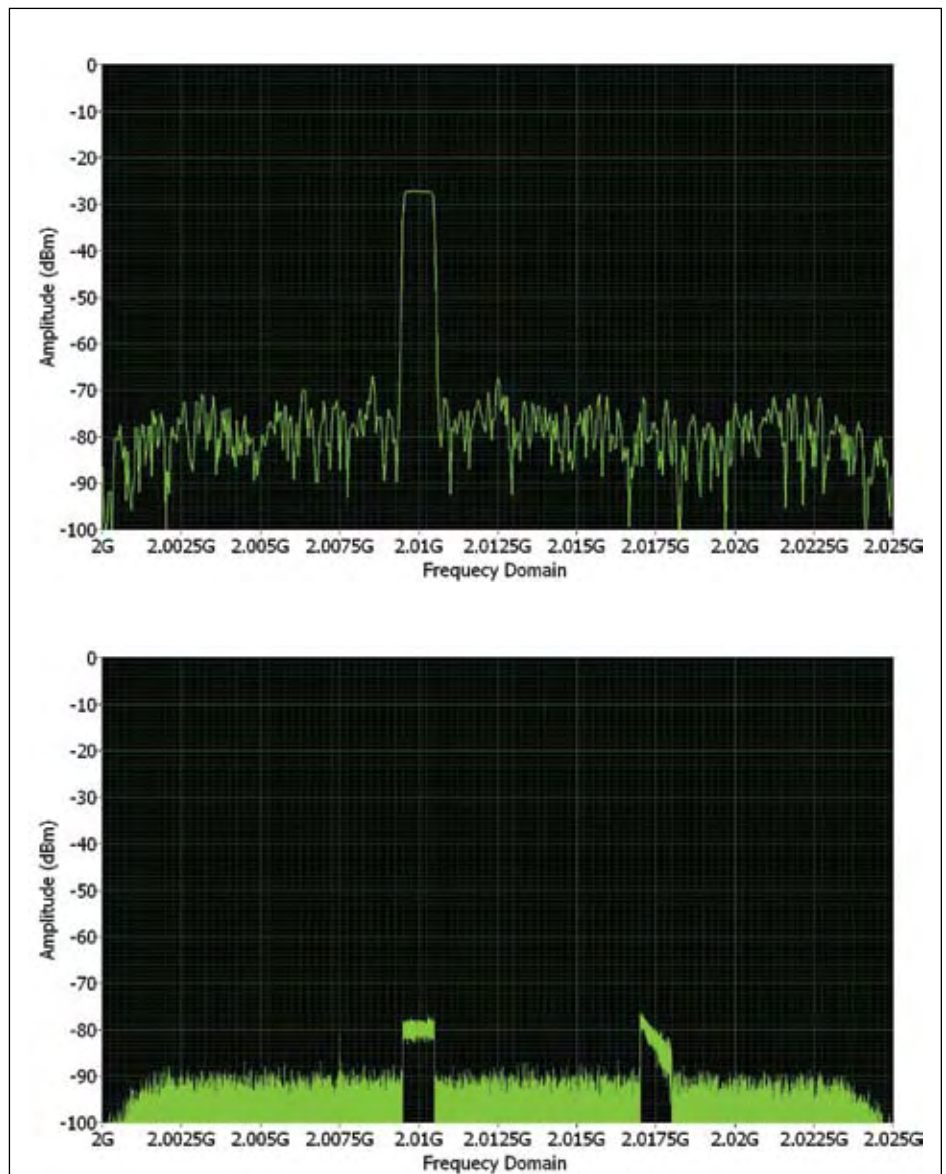
Some of the more interesting types of jamming signals are pulsed or frequency hopping signals. These types of jamming signals are generally effective and can be difficult to detect using a traditional spectrum analyzer. The difficulty lies in the need to capture both time and frequency information regarding the signal of interest. As a result, PXI stream-to-disk systems are commonly used as a method to capture a dedicated portion of RF bandwidth for several hours of time. Once recorded, we can typically use one of two methods to analyze the power, frequency and timing characteristics of jamming signals. The

two types of analysis discussed here are FFT-based analysis and joint time-frequency analysis (JTFA).

FFT-Based Signal Analysis

When performing FFT-based analysis of a jamming signal, two methods of processing can be used: in-line and post-processing. While in-line processing provides immediate results, post-processing can provide the richest set of data. Identification of subsequent jam-

ming pulses is difficult in the absence of continuous acquisition. The solution to this challenge is to record the RF data for a period of time and analyze it after the acquisition is complete. In this scenario, a chunk of RF spectrum is acquired for a long period of time and then analyzed in blocks. Using this technique, we are even able to customize the FFT size to match the duration of the pulse itself. In that situation, post-processing the data enables one to use an FFT size that can be



Figures 2 & 3

Shown here are two FFTs of the jamming burst. However, the first graph shows the use of a larger acquisition window. While a longer acquisition time reduces the RBW of the measurement, it also reduces the amplitude of the jamming pulse.

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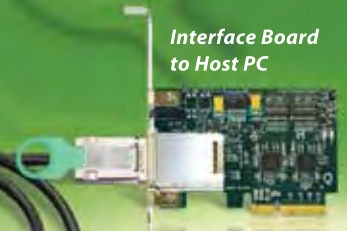
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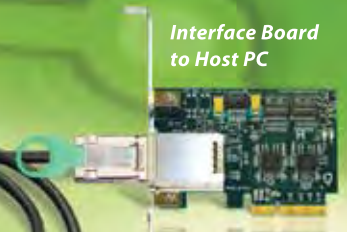
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System Development

customized according to the duration of the jamming pulse. This technique provides the most accurate method of characterizing the amplitude of the pulse because it reduces the effect of power being spread out over time.

Because the resolution bandwidth determines the acquisition time of the signal, it can affect the displayed power level of a transient signal. Because the amplitude of the burst might last as briefly as only a few microseconds, its power will be spread out over time in a long acquisition. Thus, we can more accurately characterize the frequency and amplitude of an interference signal using a short acquisition window. Figures 2 and 3 illustrate two FFTs of the jamming burst. However, the first graph shows the use of a larger acquisition window. While a longer acquisition time reduces the RBW of the measurement, it also reduces the amplitude of the jamming pulse.

As seen from that example, the ability to customize an FFT size is one benefit of performing post-analysis on a continuous RF signal. Using this technique, we are able to match the FFT window exactly with the timing of the pulse for a more accurate view of the frequency domain.

Joint Time-Frequency Analysis

A second technique used to capture both time and frequency information of interference signals is joint time-frequency analysis with a spectrogram. Similar to the FFT-based approach, the spectrogram works by performing an FFT on subsequent time-domain chunks of data. The resulting processed data can be reconstructed as a three-dimensional plot. As an example, Figure 4 illustrates the data from a spectrogram on a 3D waterfall graph. A spectrogram enables system developers to visualize a much richer set of data by displaying both power and frequency over time.

The jamming signal depicted in Figure 4 lasts for only a small period of time (approximately 25 μ sec). It transitions in frequency as well. It moves from a center frequency of 2.009 GHz to 2.016 GHz. Note that the timing information shown would not be available on a traditional spectrum analyzer, since it only captures power versus frequency. Moreover, only a stream-to-disk-based solution enables a vector signal generator to capture timing information over a long period of time.

One interesting characteristic of the jamming signal in Figure 4 is that it contains a nearly constant power over a small

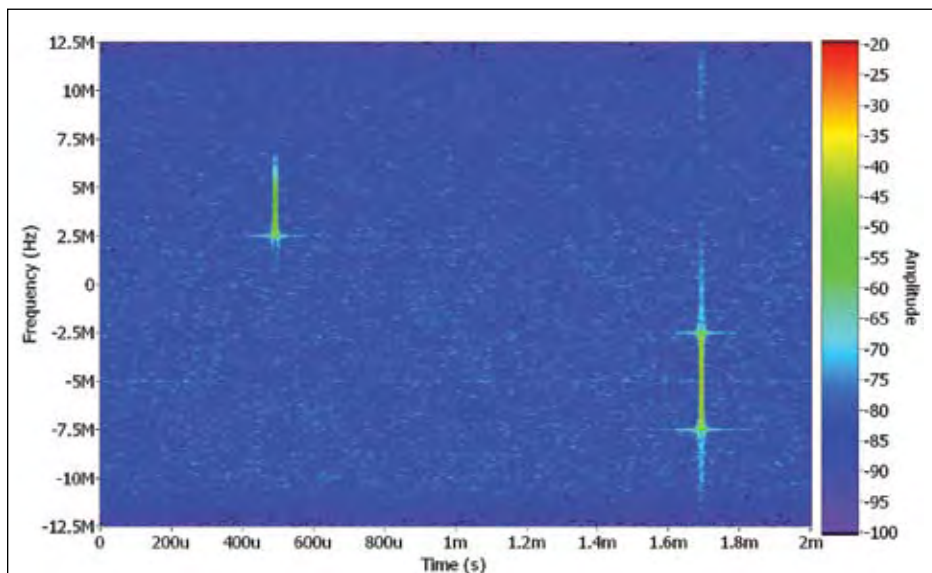


Figure 4

Shown here is the data from a spectrogram on a 3D waterfall graph. A spectrogram enables system developers to visualize a much richer set of data by displaying both power and frequency over time.

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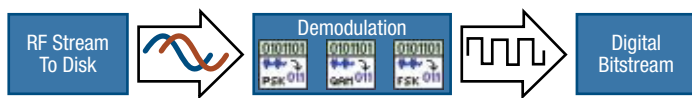


Figure 5

Using NI LabVIEW, baseband waveforms are shown here that have been stored on hard disk and can be analyzed using one of many demodulation subroutines. The diagram shows the icons for the PSK, QAM and FSK demodulation routines from the LabVIEW Modulation Toolkit.

frequency bandwidth. This characteristic lets you identify the interference as a sinc pulse that has been multiplied by a carrier. However, joint time-frequency analysis of this signal using a spectrogram provides the necessary timing information to identify characteristics such as time between pulses, pulse bandwidth and pulse amplitude.

Packet Sniffing on an Interference Signal

A second type of interference is a pirating or piggybacking communication signal. In this application, the interferer attempts to use the existing telecommunications infrastructure to transmit an illegal communications channel. As an example, an illegal transmitter might attempt to use a repeater tower to re-broadcast his custom communication channel. Because the repeater simply amplifies a specified band of spectrum, the interferer can use it to amplify his signal as well as the intended signals.

Again, "packet sniffing" a given signal can be accomplished by recording a specified bandwidth and storing it to disk. Once captured, this data can be post-processed through a variety of mechanisms. Just as with analysis of jamming signals, post analysis such as FFT and JTFA can be performed to identify frequency, power and amplitude information about the interference signal. However, for packet sniffing applications, it is common to demodulate the baseband waveform as well.

Figure 5 shows baseband waveforms that have been stored on hard disk and can be analyzed using one of many demodulation subroutines in NI LabVIEW. The figure shows the icons for the PSK, QAM and FSK demodulation routines from the LabVIEW

Modulation Toolkit. However, note that the LabVIEW modulation toolkit also offers routines for ASK, FM, AM, PM, CPM, MSK and custom demodulation. The demodulation of an unknown carrier is not trivial. In order to accurately return the bitstream of a digitally modulated carrier, it is important to know the symbol rate of the carrier. While this can be estimated by observing the channel width, it must often be determined experimentally by using symbol rates of known communication standards.

Matching with Preamble Data

By demodulating the communications signal of an interference signal, it's possible to analyze the individual bitstream being transmitted over the communication channel. In some cases, this information can be decoded by matching it with known preamble information. Typically, the greatest challenge occurs in decoding meaningful information out of a bitstream of data.

As signal intelligence applications require engineers to detect and analyze more sophisticated types of interference signals, the instrumentation requirements increase as well. Stream-to-disk systems with a vector signal analyzer enable you to capture a much richer set of data for post-analysis. As a result, we can take advantage of analysis routines such as custom FFTs, joint-time frequency spectrograms and demodulation using a variety of modulation schemes. ■■

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Technology Focus

Conduction-Cooled cPCI Boards

Maturing Conduction-Cooled cPCI Blasts Forward

Blending proven longevity and a wide infrastructure of products, conduction-cooled CompactPCI has become entrenched as a popular military embedded computing technology.

Jeff Child
Editor-in-Chief

In many markets dubbing a technology “mature” is a negative. Not so in the military. With its long development cycles, the defense industry can't risk latching onto a bus architecture that hasn't exhibited a degree of some staying power. Such caution probably kept CompactPCI from gaining any traction in mil applications until its later years when it had matured somewhat. But today, after fifteen years of maturing and proliferating, CompactPCI now boasts the elements that attract military decision makers. Among those is a vast and growing collection of cPCI products that are available from a variety of vendors in every category including single board computers, I/O boards, slot-card power supplies, storage subsystems, mezzanine carriers, DSP engines and many others.

Over the past several years, an expanding set of conduction-cooled CompactPCI boards has emerged, some even from outside the usual crowd of conduction-cooled board makers. The “Conduction-Cooled cPCI Boards Roundup” on the following pages showcases some examples of such products.

cPCI never did achieve the explosive adoption in telecom that many had envisioned. Yet it does enjoy a solid piece of the overall embedded board market. Meanwhile, the PCI Industrial Manufacturers Group (PICMG) continues to develop performance upgrade paths for cPCI, such as PICMG 2.16 and CompactPCI Express. All these factors lead to a perception that cPCI will be around for the long haul—an essential characteristic in order for its adoption in military and other high-reliability, long life-cycle applications.

In the past year a growing number of vendors have announced military and aerospace design wins for their conduction-cooled cPCI products. And considering that many such wins aren't made public, it's clear that cPCI is enjoying a lot of adoption in military and aerospace system designs. Earlier this year Aitech Defense Systems' 3U CompactPCI boards were launched on board a pair of spacecraft tasked to demonstrate fully autonomous on-orbit spacecraft servicing capabilities. Launched in early March of this year, Orbital Express (Figure 1) is part of a DARPA program that consists of two spacecraft: the Autonomous Space Transport Robotic Operations (ASTRO) vehicle, developed by Boeing; and NextSat, a prototypical modular next-generation serviceable cli-



Figure 1

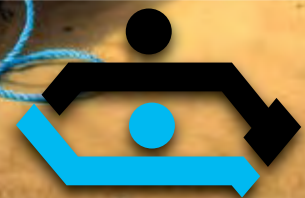
CompactPCI is used in the Autonomous Space Transport Robotic Operations (ASTRO) satellite. Shown here, an Atlas V rocket blasts off from Cape Canaveral on March 8 carrying Orbital Express, which is comprised of two satellites: the ASTRO service vehicle, and the Next-Generation Serviceable Satellite (NextSat).

ent satellite developed by Ball Aerospace. The ASTRO computers (AC-1, AC-2 and AC-3) are integrated as three subsystems and are based on Aitech's new 3U CompactPCI-based product line including the PowerPC-based 3U S950 SBC, various analog and digital I/O boards.

CompactPCI also achieved a win in the U.S. Army's Non-Line-Of-Sight Launch System (NLOS-LS) platform. The NLOS-LS is part of “spin-out one” within the Army's Future Combat Systems (FCS) program. NLOS-LS is being developed for the U.S. Army by Netfires LLC, a joint venture between Lockheed Martin and Raytheon. The cPCI processing subsystem from GE Fanuc Embedded Systems was selected by Lockheed Martin for the program. The subsystem comprises an adapted version of one of the GE Fanuc company's standard rugged enclosures, together with a Compact PCI 6U CP1A single board computer fitted with some I/O and networking PMC modules. ■■

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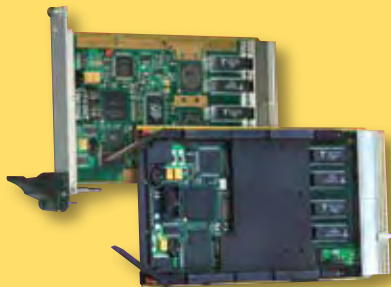
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Technology Focus:

Conduction-Cooled cPCI Boards Roundup

PowerPC SBC Series Is Rich with I/O

The 3U form-factor has become the CompactPCI flavor of choice for space-constrained applications. No other standard form-factor permits such high levels of compute and I/O densities. ACT/Technico's offerings in this space are its 680x series of conduction-cooled 3U CompactPCI SBCs. Based on the Freescale MPC7447/7448 processor, the boards



are ideal for a wide range of rugged, embedded applications including ground mobile, shipboard, airborne and homeland security.

These new processor boards are designed around Freescale's PowerPC e600 processors, the MPC7447A at 1 GHz or the MPC7448 at 1.4 GHz. The 680x boards integrate numerous I/O: two Gigabit Ethernet channels, two high-speed USB 2.0 ports, two multi-purpose serial controllers and two high-speed ports. The boards support up to 512 Mbytes of DDR ECC SDRAM, 128 Kbytes of ultra-fast SRAM and 64 Mbytes of flash EPROM. A 64-bit PMC card can be added via a single PMC expansion slot. Designed to meet the most severe environments, the boards are available in standard and extended temperature ranges, in addition to the conduction-cooled version. 680x series software is based on UBOOT, along with a comprehensive power-on Built-in-Test (BiT). Board Support Packages (BSPs) are available for VxWorks and Linux. Pricing for the 680x series starts at \$3,063 in low quantities.

ACT/Technico
Warminster, PA.
(215) 956-1200.
[www.acttechnico.com].

24W 3U cPCI SBC Is Low Power Solution

CompactPCI, particularly in its 3U flavor, has earned acceptance among military designers. Continuing to feed those demands, Aitech Defense Systems announced two power-saving, rugged 3U CompactPCI single board computers with improved processing performance of up to 1.4 GHz and broader memory and I/O options. The Aitech C901 SBC and its low-power version, the C901L, feature Freescale 7448 PowerPC processors with on-chip L1 and enhanced L2 caches and AltiVec Technology. A fully populated C901 with 512 Mbytes of DRAM operates at a typical power consumption of 24.0W 1.4 GHz processor speed. The C901L version reduces that power consumption to less than 17.0W (at 1.0 GHz) for applications where power dissipation concerns are more critical than processor speed.

Both board configurations provide up to 1 Mbyte on-chip cache memory, 200 MHz



memory buses and 2 Gbytes of flash memory. They also offer six standard variants of I/O capabilities including multiple choices of Gbit Ethernet ports, Fast Ethernet ports, USB ports, high-speed serial ports and up to eight discrete I/O channels. An industry-standard PMC slot allows for installation of additional modules and functionality. Available in both rugged conduction-cooled and air-cooled formats, pricing for the C901 starts at \$5,300.

Aitech Defense Systems
Chatsworth, CA.
(888) 248-3248.
[www.rugged.com].

Board Blends FPGA and Four TigerSHARC DSPs

FPGAs and DSPs working together form a powerful weapon for advanced signal processing applications. Exemplifying that trend is BittWare's GT-3U-cPCI (GT3U), a ruggedized 3U CompactPCI board that has been designed for demanding multiprocessor-



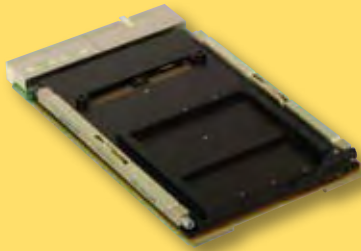
based applications. The GT3U features a large Altera Stratix II GX FPGA, one cluster of four ADSP-TS201S TigerSHARC processors from Analog Devices, a front panel interface supplying four channels of high-speed SerDes transceivers, and a back panel interface providing RS-232/RS-422 and 10/100 Ethernet. Simultaneous on-board and off-board data transfers can be achieved at a rate of 2 Gbytes/s via BittWare's ATLANTiS framework implemented in the Stratix II GX FPGA. The board also provides a large amount of onboard memory including 1 Gbyte of DDR2 SDRAM or 64 Mbytes of QDR SDRAM, as well as 64 Mbytes of flash memory for booting the FPGA and DSPs.

The GT3U features a single cluster of four ADSP-TS201S TigerSHARC DSPs, which are interconnected by a 64-bit cluster bus running at up to 100 MHz. The ADSP-TS201 processor operates at up to 600 MHz, providing 3.6 GFLOPS of peak processing power. Because of its superscalar architecture, the ADSP-TS201 is also efficient at fixed-point processing, with each DSP supporting 14.4 Bops of processing. Along with 24 Mbits of on-chip RAM, each DSP also boasts four high-speed LVDS link ports. Each full-duplex link port is comprised of a 4-bit transmit and a 4-bit receive channel, and can support up to 500 Mbytes/s in each direction for a total maximum throughput of 1 Gbyte/s.

BittWare
Concord, NH.
(603) 226-0404.
[www.bittware.com].

1.5 GHz Core 2 Duo Board Supports XMC

Mezzanine expansion remains a popular strategy for mixing and matching specific I/O needs in military systems. Concurrent Technologies has introduced a low-power, conduction-cooled, 3U CompactPCI SBC called the TP 402/351-RC that uses the latest mobile dual-core processor and server chipset from the Intel embedded roadmap. It combines the performance of the 1.5 GHz Intel Core 2 Duo processor with the Intel 3100 server chipset interfacing up to 2 Gbytes of soldered DDR2 ECC SDRAM.



This ruggedized SBC supports an XMC module in a single slot, and can operate in a system slot, peripheral slot or as a blade. The TP 402/351-RC is well suited to conduction-cooled applications within the telemetry, defense, security and aerospace markets. A ruggedized air-cooled version and a range of commercial extended temperature versions are also available. The board also supports, in a single slot, an XMC site (via a x4 PCI Express port), and can operate as a system controller for up to 7 peripheral boards including hot-swap control, or can operate in peripheral slot or as a blade. For fast external control and high-speed data paths, the TP 402/351-RC provides two high-speed USB 2.0 ports, one RS-232/422/485 and one RS-232 port, plus the Intel 82571EB dual Gbit Ethernet controller (with a x4 PCI Express port) that can sustain data rates of up to 4 Gbits/s via the two Gbit Ethernet interfaces.

Concurrent Technologies
Woburn, MA.
(781) 933 5900.
[www.gocct.com].

3U Board Features Flexible I/O Scheme

Space and weight constraints for embedded technology in military and aerospace applications have created difficult compromises between size and a full complement of I/O. The SCP/DCP-124P from Curtiss-Wright Controls Embedded Computing takes advantage of the compact 3U CompactPCI SBC format and I/O flexibility to overcome these challenges. Utilizing PICMG 2.3, the SCP/DCP-124P routes I/O signals and supports mapping of PMC I/O through the backplane. It features Freescale's AltiVec-enhanced 7448 PowerPC supported by 1 Mbyte of internal ECC L2 cache running at core processor speed and up to 1 Gbyte of ECC DDR SDRAM.

The board's cPCI bus operates at 33/66 MHz and supports both 3.3V and 5V signaling. System expansion is provided by an onboard 64-bit, 100 MHz PCI-X-capable PMC site. The SCP/DCP-124P is available in both conduction-cooled and air-cooled versions with optional rear transition cable sets to facilitate system integration and development. Conduction-cooling is rated up to -40° to +85°C (Level 200). Ruggedization levels available include L0, and L100 air-cooled, and L100 and L200 conduction-cooled. Storage temperature is -50° to +100°C, and humidity rating is 10 to 95 percent RH non-condensing. Software support includes BSPs for VxWorks

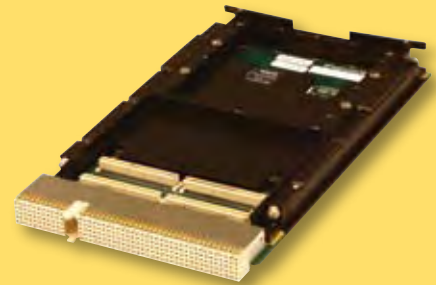


5.5.x/Tornado 2.2.x and 6.x/Workbench 2.x for PowerPC, CWCEC Linux and Integrity. Support is also provided for SSSL, Curtiss-Wright's AltiVec-optimized signal processing library. Pricing starts at \$6,030.

Curtiss-Wright Controls
Embedded Computing
Leesburg, VA.
(703) 779-7800.
[www.cwcmbedded.com].

Dual PA Semi Cores Climb Aboard 3U cPCI

Compute density has become the watchword for a variety of advanced military programs, such as UAVs, next-gen military vehicles and so on. Serving just such needs, the PA Semi processor architecture is beginning to make a significant presence in the embedded computing realm. Extreme Engineering's new XPedite8030, a 3U CompactPCI single board computer for ruggedized systems, sports two PA Semi PA6T cores running at up to 2.0 GHz



while dissipating less than 17W. The PA6T-1682 delivers optimum performance-per-watt. The PA Semi PA6T-1682 PWRficient integrated platform processor combines dual PA6T cores with high-performance communication to two DDR2 SDRAM channels and a plethora of network interfaces.

The XPedite8030 supports two separate channels of up to 1 Gbyte each of DDR2 ECC SDRAM, as well as up to 1 Gbyte of NAND flash. The Gigabit Ethernet or dual Fast Ethernet, GPIO, I2C, PMC I/O, XMC I/O, dual USB ports and dual RS-232/RS-422 ports are available through the J2 connector. XPedite8030 can be built as a system or peripheral cPCI module. To the system designer, the XPedite8030 provides a feature-rich solution to support the next generation of rugged embedded applications. Both a VxWorks Board Support Package (BSP) and a Linux 2.6 LSP are available.

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3U Core Duo LV Board Serves Upgrade Role

Technology upgrades are a key part of any military system life cycle. Feeding such needs, GE Fanuc Embedded Systems offers the CR5 rugged 3U CompactPCI single board computer. Based on an Intel Core Duo LV (low voltage) processor operating at up to 1.66 GHz, the CR5 is designed for a broad range of applications, with a conduction-cooled option making it especially appropriate for military applications in harsh environments. The CR5 supports up to 2 Gbytes of DDR2 SDRAM with ECC on a 400 MHz memory bus, and features two Gbit Ethernet ports, two SATA ports, two USB 2.0 ports and eight GPIO ports.

The Core Duo processor provides two complete execution cores in a single processor package, sharing a 667 MHz front side bus and 2 Mbytes of L2 cache for maximum performance and application productivity, but with low power consumption. Also featured by the CR5 is the Intel 3100 ICH integrated memory and I/O controller hub, which



provides two USB 2.0 ports, two SATA ports and a standard COM port. An optionally available daughter card for the CR5 provides support for a CompactFlash module and SVGA graphics. The CR5, which is PICMG 2.0- and VITA 47-compliant, provides operating system support for VxWorks, Linux and Windows XP.

GE Fanuc Embedded Systems
Charlottesville, VA.
(800) 368-2738.
[www.gefanucembedded.com].

6U Core 2 Duo Board Boasts Full Health Monitoring

An increasing number of military applications are requiring computing that can operate autonomously. That means the system has to monitor its own health. With that in mind, General Micro System's "2nd Coming" is the industry's first 6U, Core 2 Duo, Conduction-Cooled cPCI SBC to provide full System Health Monitoring and reporting to meet all PICMG 2.9 specifications, while adding a slew of additional health monitoring and reporting system status to an external device.

The C276 supports up to 4 Gbytes of 667



MHz DDR-2 memory and vast onboard I/O. The standard I/O included are dual Gbit Ethernet on PCI-e bus with TCP/IP Offloading Engine, dual IDE, quad SATA with RAID (0, 1, 5, 10 and 50) capabilities, five USB-2.0, 1 Mbyte of user/Boot flash and two serial ports. Additional standard I/O included are: one PMC/XMC site with rear I/O, 16 bidirectional Digital I/O lines and dual COM ports with RS-232/422 buffers (jumper selectable). The C276 module is fully compliant to IEEE Std. 1101.2 and ANSI/VITA 2-0 2001. The 2nd Coming operates from -40° to +85°C at the rails with relative humidity of 5-95 percent at 40°C, and may be exposed to shocks of up to 100g for 5 ms, or 40g for 11 ms in 3 axis. The 2nd Coming supports extremes, vibrations range from 5 Hz to 2 KHz for up to 30 minutes at 15 gRMS in each axis.

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(909) 980-4863.
[www.gms4sbc.com].

Dual 1.4 GHz PowerPCs Ride 6U CompactPCI

CompactPCI has passed the test of longevity and maturity, making it one of the accepted form-factors in today's military applications. Feeding that trend, Interface Concept has unveiled a high-performance 6U CompactPCI board, the IC-xe6-cPCIb, powered by one or two Freescale 1.4 GHz MPC7448 PowerPC processors. This new single or dual processor SBC is PICMG2.16-compliant and blends low power consumption and large communications capabilities. The board implements a Marvell Discovery III chipset (MV64460).

The memory banks are made of up to 2 Gbytes of DDR-ECC SDRAM, up to 256 Mbytes of mirror flash and up to 1 Gbyte of soldered NAND flash. A quad UART provides four additional asynchronous channels available on P2 connector. The 64-bit PCI/PCI-X bridge allows the IC-xe6-cPCIb to handle two PMC slots with PnIO routed to J3/J5. Thanks to its



SATA controller, the IC-xe6-cPCIb can manage directly four storage devices. The IC-xe6-cPCIb provides one Gbit Ethernet, one console, one USB-2 and two SATA ports on the front panel. This board has been designed to meet the most severe environments—standard, extended and rugged grades. Prices start at \$3,950.

Interface Concept
Briec de l'Odet, France.
+33 (0)2 98 57 30 30.
[www.interfaceconcept.com].



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6U SBC Sports 2 GHz Pentium M CPU

Military and aerospace applications such as aircraft monitoring, visualization and control all have something common. They demand a blend of high-performance compute muscle, with a ruggedness suited to harsh environments. Along those lines, MEN Micro offers an Intel-based conduction-cooled cPCI SBC that employs a low-power Pentium M processor operating at up to 2 GHz and a 915GM chipset. Called the D601, this 6U card components are soldered directly to the board, eliminating the need for socketed components and providing exceptional temperature, shock



and vibration properties according to the current DIN, EN and IEC industry standards.

In addition, the versatile SBC only needs one bus slot and can be used in fanless embedded computing systems. Other Intel processors, such as the low-voltage 1.4 GHz Pentium M or the ultra-low-voltage 1 GHz Celeron M, can be used on the D601, enabling operation at an extended temperature range of -40° to +85°C (-40° to +185°F). The board's rear I/O includes graphic support via VGA connectors for display of the same or different images on several monitors, two Gbit Ethernet interfaces connected via PCI Express and three USB 2.0 interfaces. The board also features two SATA interfaces for mass storage connection, and a PATA to connect a robust IDE-driven CompactFlash device, providing nearly unlimited space for user applications. Pricing for the D601 is \$6,644.

MEN Micro
Ambler, PA.
(215) 542-9575.
[www.menmicro.com].

FPGA-Based Multicomputer Board Goes Rugged

Military designers creating small, portable systems for C4ISR electronic warfare, signals intelligence (SIGINT), synthetic aperture radar (SAR) and electro-optic/infrared (EO/IR) applications need lots of digital signal processing power in a minimum-sized package. With that in mind, Mercury Computer Systems' MCP3 FCN module is a rugged 3U CompactPCI digital signal processor. This conduction-cooled module is designed for deployment in harsh environments and to withstand high heat, humidity, shock and vibration. The MCP3 FCN is a multicomputer system module that integrates a 1 GHz Freescale MPC7447A PowerPC processor, a Virtex-II Pro P40 FPGA and a PMC site.

The MCP3 FCN's flexibility extends to multiple I/O options. A direct connection to the FPGA, using the J2 pins of the cPCI connector, enables high-speed digital intermediate frequency (IF) I/O. In addition, industry-standard PMCs, such as the dual-channel digital receiver PMC configured with early test systems, can be attached directly to the board. A PCI bus connection is available via the J1 pins of the CompactPCI connector.

For those parts of the application that will run on the FPGA, developers can use Mercury's FPGA Developer's Kit (FDK), which comprises a collection of Mercury-



developed IP, build files, command line tools, libraries, headers, drivers, board descriptors, diagnostics and consulting support, all focused on helping engineers efficiently create reliable applications. OEM pricing for the MCP3 FCN module starts at \$20,000.

Mercury Computer Systems
Chelmsford, MA.
(978) 256-1300.
[www.mc.com].

3U PowerPC SBC 3U cPCI Aims at Tactical Apps

In avionics and defense vehicles, storage, networking and imaging applications demand high-performance, compact, real-time systems. The compute engine driving those systems must share these same characteristics. The PowerEngineC7 3U CompactPCI SBC from Thales Computers was designed with those applications in mind. The PowerEngineC7 is the first member of the company's family of rugged 3U CompactPCI embedded computers



for military and aerospace applications.

The PowerEngineC7 is based on IBM's 800 MHz PowerPC 750GX dual issue, superscalar control processor. The 32 Kbyte L1 cache has a 32-byte line, an 8-way set associative instruction cache and a 32 Kbyte, 32-byte line, 8-way set associative data cache. The 1 Mbyte internal L2 cache has ECC clocked at processor frequency. Up to 512 Mbytes of DDR SDRAM with ECC supports code execution copied from flash memory, and is soldered to the board for increased ruggedization. The board includes 64 Mbytes of system flash, 128 Mbytes of user flash, a dual Ethernet 10/100 port and dual serial lines. The IEEE P1386/1386.1 PMC expansion slot has a 32-bit 33/66 MHz PCI bus interface. A predefined area of the memory is protected from PCI and Ethernet accesses and allows the definition of a dedicated PPC communications area. The PowerEngine C7 is rugged conduction-cooled (-40° to +85°C), and it supports VxWorks 5.5.1 for Tornado 2.2.1. Pricing starts at \$4,450 in single quantities.

Thales Computers
Edison NJ.
(732) 494-1011.
[www.thalescomputers.com].



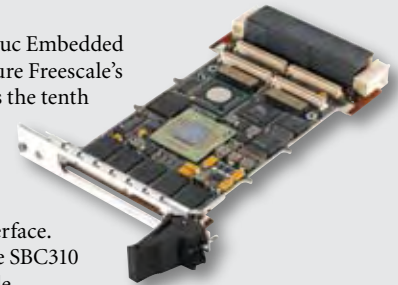
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Products

3U VPX Card Sports Dual Core PowerPC 8641D

This year has been shaping up as the “year of VPX products” as board vendors expand their VPX offerings. GE Fanuc Embedded Systems has announced the SBC310 3U VPX single board computer—the first 3U VPX single board computer to feature Freescale’s dual core PowerPC 8641D and to provide support for a PMC/XMC site. With up to 1 Gbyte of SDRAM, the SBC310 is the tenth member of the GE Fanuc Embedded Systems family of VPX products. The SBC310 is optionally available in any of five ruggedization levels, making it suitable for deployment in the harshest environments.

The SBC310 features two 4-lane PCI Express ports across the backplane, providing high-speed data communication to other system elements. It also provides a number of high-speed interfaces for off-board communication, including two 10/100/1000 Base-T Gbit Ethernet ports, two USB 2.0 ports and a Serial ATA disk interface. In addition, there is support for legacy interfaces, including two RS-232 ports and four general-purpose I/O lines. The SBC310 utilizes state-of-the-art cooling technology to allow a PMC or XMC to be fitted without compromising processor node performance.



GE Fanuc Embedded Systems, Charlottesville, VA. (800) 368-2738. [www.gefanucembedded.com].

PIC24 Microcontrollers Get ThreadX RTOS Support

Nanocomputing has become an important technology trend in military system designs. As a result, demand is on the rise for sophisticated multithreaded software on ultra small form-factor platforms. Taking aim at that arena, Express Logic has made available Express Logic’s new ThreadX Microcontroller Edition RTOS for the 16-bit PIC24 microcontrollers (MCUs) and dsPIC digital signal controllers (DSCs) from Microchip Technology.



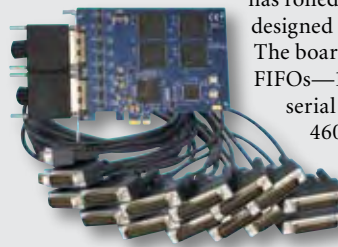
Until now, ThreadX has been available only for 32-bit processors and DSPs. ThreadX/MCU is a fully upward-compatible, reduced-size, fine-tuned 16-bit edition of Express Logic’s popular 32-bit ThreadX RTOS and is available exclusively for Microchip’s 16-

bit PIC24 MCUs and dsPIC30/33 DSCs. ThreadX/MCU provides full preemptive scheduling, interrupt management, message passing, thread synchronization, resource locking, event management and timer control; and supports up to 10 threads, queues, timers, mutexes, event flag groups, block pools and byte pools. ThreadX/MCU is designed to work with Microchip’s powerful and affordable MPLAB development tools. ThreadX/MCU, NetX/MCU, FileX/MCU and PEGX/MCU are available immediately in full production licenses beginning at \$5,990. Demo licenses are available free of charge.

Express Logic, San Diego, CA. (858) 613-6640. [www.expresslogic.com].

PCI Express Board Serves up 16 RS-232 Ports

PCI Express was by no means the first switched fabric technology to come on the scene, but it has definitely captured the widest adoption, in the both military and general embedded applications. Sealevel Systems



has rolled out a 16-port RS-232 serial I/O adapter designed for the new PCI Express bus design. The board uses 16C854 UARTs with 128-byte FIFOs—16 times larger than other boards. Each serial port provides a maximum data rate of

460.8 Kbits/s, and the COMM+16.PCIe has an operating range from 0° to +70°C.

Extended temperature versions operating from -40° to +85°C are available. All Sealevel I/O products have a lifetime warranty.

The COMM+16.PCIe is ideal for connecting to PLCs, bar code readers, scales and other data acquisition/control devices using the included DB-25M fan-out cable (DB-9M fan-out cable available as an option). The product includes SeaCOM software for Windows 98/ME/NT/2000/XP/Vista and Linux operating systems. As an added value, customers also receive WinSSD, a full-featured application for testing and diagnostics including BERT (Bit Error Rate Testing), throughput monitoring, loopback tests and test pattern message transmissions. The COMM+16.PCIe standard price is \$679 and product is available for shipping.

Sealevel Systems, Liberty, SC. (864) 843-4343. [www.sealevel.com].

LXI Triggering Box Does Precise Synchronization



LXI, the LAN-based successor to GPIB, offers flexible packaging, high-speed I/O and prolific use of LAN across a broad range of aerospace and military applications. Agilent Technologies has introduced the world’s first LXI trigger box that enables precise synchronization over LAN for LXI Class C and GPIB instruments, elevating their performance to LXI Class B standards. When an LXI Class C or GPIB instrument is connected to the Agilent E5818A LXI trigger box, it gains the timing capabilities of an LXI Class B instrument. Leveraging the IEEE 1588 precision time protocol (PTP) synchronization, the trigger box enables sub-nanosecond time triggering and time stamping of events for the attached instruments. With reliable event-log data, users can trace and troubleshoot faults easily.

The Agilent E5818A LXI trigger box is a stand-alone LXI Class B device. It can achieve a synchronization accuracy of up to 13 ns (standard deviation over direct connection) and provide time stamping of up to 5,000 events. Each trigger box provides BNC connectivity to two instruments (any combination of GPIB or LXI Class C). The Agilent E5818A LXI trigger box is available now and is priced at \$1,500.

Agilent Technologies, Santa Clara, CA. (877) 424-4536. [www.agilent.com].

Managed Fiber Ethernet Switch Supports SNMP

Everything Over IP (EOIP) is the direction the military is heading and that means a growing demand for Ethernet network switch gear. Aaxeon Technologies has released its Lanolinx line of Fiber Ethernet Switches. The Lanolinx Fiber Ethernet Switches include 100FX and Gigabit Fiber models, supporting multimode or single mode fiber. These switches also have up to 24 10/100 Copper ports. In addition, models are available with two fiber ports instead of one.

The units support IEEE 802.3/802.3u, store-and-forward switching and IP Security. The 10/100, Full/Half Duplex switches have MDI/MDI-X auto-sensing, Rate Limiting and support both SNMP/Telnet/Console/Web management and port-based VLAN / 802.1 Q Tag VLAN. Offered in a rack-mountable enclosure, the switches provide IEEE 802.1p Class of Service and Port base, Tag base and Type of Service priority method. IGMP with Query mode for multimedia and port mirroring are supported as well. Pricing for the 24-Port SNMP Managed Fiber Switch starts as low as \$289.

Aaxeon Technologies, Brea, CA. (714) 671-9000. [www.aaxeon.com].



Hybrid Cables Target Military Shipboard Apps

The drive in military shipboard computer these days is toward simplicity and cost reduction. Gone are the days when the Navy tolerated a zillion different cable types cluttering up a vessels superstructure. Satisfying such needs, Tyco Electronics has developed military hybrid cables that combine multiple components under one single jacket, which cuts down on cable weight and physical space requirements enabling a faster and more cost-effective install.

Tyco Electronics offers a full range of customized cable designs that will utilize MIL-DTL-24640-compliant materials, and when required, an optimized shield design for harsh EMI environment requirements. Hybrid shipboard cables may incorporate innovative waterblocking tapes and yarns or traditional physical waterblocking solutions to prevent the ingress of water during operation. Designers can select from a wide range of standard or specialized components and may incorporate controlled electrical, signal and power components into a single optimized design intended to deliver consistency and quality. Components can include SAE-AS-81044, MIL-W-22759, MIL-DTL-24643/59-/61, 100BaseT, IEEE 1394 and RG lightweight alternatives. Prototype samples are available upon request.

Tyco Electronics, Berwyn, PA. (610) 893-9800 [www.tycoelectronics.com].



5-Port Gbit Ethernet Switch Operates at -10° to 60°C

The military continues to warm to Ethernet. Few network technologies can boast the longevity and ubiquity of the technology. With its latest rugged Ethernet product, the eAutomation Group of Advantech has introduced the EKI-2725 5-port unmanaged industrial Ethernet switch featuring full Gbit capacity for bandwidth-intensive applications. The EKI-2725 is equipped with five 1000Base-T Gbit Ethernet ports and supports 9k Jumbo Frames, which allows larger blocks of data to be sent with each transmission, for increased network throughput and reduced CPU utilization of connected devices.

Designed for the harsh environment of industrial applications, the EKI-2725 is packed in a compact metal DIN rail-mount chassis built to withstand shock and vibration. The EKI-2725 features 4,000 VDC Ethernet ESD protection, power line surge (EFT) protection of 3,000 VDC and an operating temperature of -10° to 60°C. The EKI-2725 includes dual 12 to 48 VDC power inputs for redundant power configurations to ensure system uptime. In the event of a problem with external power, a built-in fault relay is available to signal an external programmable logic controller (PLC) or controller. The EKI-2725 5-port Gbit Ethernet switch is priced starting at \$275.

Advantech, eAutomation Group Cincinnati, OH. (800) 205-7940. [www.eAutomationPro.com].



AMC Load Board Aids MicroTCA System Debug

The military market is well into the evaluation and “kicking-the-tires” stage for MicroTCA and AMC. Helping system designers to test and debug their MicroTCA prototype systems, Elma Electronic has released a new AMC Load Board. The Advanced Mezzanine Card (AMC) Load Board is compliant to the MicroTCA.0 and AMC.0 Advanced Mezzanine Card specifications. The unit comes standard in the single module/full size with options for double modules and compact or mid-sizes. Hot-swap pluggable, the board incorporates a JTAG interface and IPMI support.

The load board is configurable to seven wattages: 0W, 20W, 30W, 40W, 50W, 60W and 70W. Six LEDs on the front panel indicate which power level is activated. Custom wattages and access management is available upon request. The power level can be changed by repeatedly pressing the front panel button, cycling through all power levels. The load board has three temperature sensors; one on the bottom and two on the top. These are implemented as IPMI temperature sensors and could be read through the MicroTCA Carrier Hub (MCH). The unit also features redundant operation with automatic switchover. Pricing for the AMC Load Board is under \$300 depending on volume.

Elma Electronic, Fremont, CA.
(510) 656-3400. [www.elma.com].

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COTS Products

14-Slot 3U PXI Chassis Is Portable

When a military test system is integrated enough to be portable, the nature of what it can do changes dramatically. An example along such lines is ADLINK Technology's new PXIS-2690P—a 14-slot, 3U portable PXI chassis fully compliant with the PXI specification, rev. 2.2. The PXIS-2690P is designed for military, aero-defense, field testing and in-vehicle testing applications by providing a touch panel 15" LCD display, keyboard, touchpad, DVD combo drive and 500W power supply in an aluminum alloy frame.

Designed for ruggedness and stability, the PXIS-2960P has been fully tested for a variety of shock and vibration situations—such as those experienced in outdoor applications. Three onboard 120 mm x 120 mm x 25 mm fans deliver an airflow rate of 223.5 cfm to help ensure proper operation even in high-temperature environments. The 13 peripheral slots of the PXIS-2690P support a variety of 3U PXI/CompactPCI modules such as digitizers, waveform generators, multimeters, data acquisition cards, analog output cards and digital I/O cards. The PXIS-2690P is available now, priced starting at \$6,450, and is available with discounts in volume.

ADLINK Technology America Irvine, CA. (949) 727-2077.
[\[www.adlinktech.com\]](http://www.adlinktech.com).



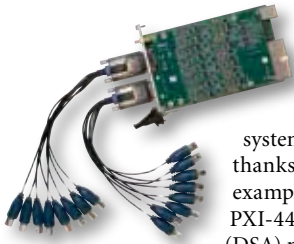
Expandable Rugged Box Can Take the Heat



The military is embracing the trend toward stand-alone rugged boxes with full force. Feeding those needs, Octagon Systems has announced the RMB-S CORE, a high-performance mobile server, the latest member of its CORE SYSTEMS line of rugged systems with expandable I/O and fanless operation. The RMB-S is a "no compromise" design that optimizes the electrical, thermal and mechanical components for maximum reliability.

The basic unit includes the processing power, mobile power supply, memory, connector card and I/O for most applications. Standard I/O includes dual Ethernet, quad USB 2.0, dual serial, CRT & LCD video and digital I/O. The RMB-S is fully functional out-of-the-box, and additional I/O, such as GPS, analog, radio or Wi-Fi, can be readily added via PC/104 and PC/104-Plus modules. An option panel can be easily removed and punched for custom annunciators, connectors and controls. Heat from the system is channeled directly to the case to help prevent internal hot spots. The RMB-S mobile server operates in ambient temperatures from -40° to 70°C, depending upon the processor speed, user options and mass storage devices. A MIL-810F version offers a case with military-grade connectors and gasket sealing to provide dust-resistant, waterproof protection in outdoor environments.

Octagon Systems, Westminster, CO. (303) 430-1500.
[\[www.octagonystems.com\]](http://www.octagonystems.com).



PXI Card Packs in Sixteen 24-Bit Data Acq Channels

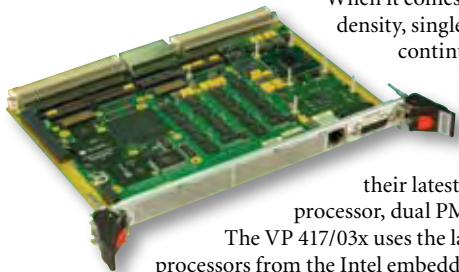
Military system designers now can easily build complex, synchronized systems for high-channel-count applications thanks to a new crop of integrated PXI systems. An example along those lines is National Instruments' PXI-4498 and PXI-4496 dynamic signal acquisition (DSA) modules, which offer 16 simultaneous

24-bit analog inputs per module and IEPE constant current signal conditioning for precision measurements with microphones and accelerometers in high-channel-count systems, such as noise mapping, beamforming applications and structural vibration.

The NI PXI-4498 features four analog input voltage ranges, while the NI PXI-4496 has two analog input voltage ranges. With 16 simultaneous channels in a single PXI module, these are the most dense DSA modules from NI. Engineers can use the modules with an 18-slot PXI chassis to hold 272 synchronized channels in a single chassis and more than 13,000 synchronized channels in a distributed PXI system. The modules feature a maximum sampling rate of 204.8 ksamples/s per channel and include TEDS smart sensor support for error free setup. Pricing for the PXI-4498 and PXI-4496 DSA modules starts at \$7,999.

National Instruments, Austin, TX. (512) 683-0100. [www.ni.com].

Core2 Duo Rides VME Dual PMC SBC



When it comes to bumping up compute density, single board computer vendors continue to push the envelope of what can be done in single slot card. Exemplifying that trend, Concurrent Technologies has released their latest single-slot VME dual-core processor, dual PMC, single board computer.

The VP 417/03x uses the latest mobile dual-core processors from the Intel embedded roadmap, the 1.5 GHz or the 2.16 GHz Intel Core 2 Duo processor. The VP 417/03x family is I/O-compatible with the popular and long-standing VP 31x/02x family and gives an even greater improvement in measured performance/watt. The board is ideal for low power intensive processing applications where the dual processor cores can access up to 4 Gbytes on board DDR2 ECC SDRAM at up to 6.4 Gbytes/s.

With two 66 MHz PMC sites, suitable for a wide range of PMC modules, the board also includes extensive I/O functionality and can support VITA 31.1. Commercial and extended temperature versions are now available and ruggedized, conduction-cooled or air-cooled versions will be available shortly. VITA 31.1 Gigabit Ethernet on a VME64x backplane enables a tried and tested method of implementing a LAN-based multiprocessor architecture by leveraging readily available Ethernet hardware, TCP/IP software, clustering and other network management tools.

Concurrent Technologies, Woburn, MA. (781) 933 5900. [www.gocct.com].



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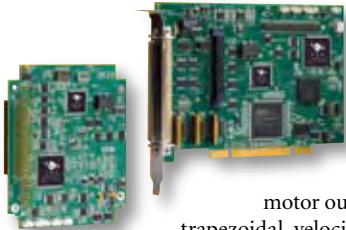


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Motion Control Cards Deliver High-Speed Trace



The priority for military motion control systems is smaller, high-precision motors and more of them. Feeding that trend, two motion control cards from Performance Motion Devices provide real-time, high-speed servo trace capture with 40 Kbytes onboard dual-port memory. This trace feature allows up to four motion variables to be stored at the same time. Each variable can be either 16 or 32 bits in size.

Designed with PMD's Magellan Motion Control IC, the Prodigy Motion Cards provide board-level, multi-axis motion control for DC brush, brushless DC, step and microstepping motors. They are available in PCI and PC/104 configurations, and provide 1, 2, 3 or 4 axes of control. In addition to trace capture, Prodigy cards provide motion control features including trajectory generation, servo loop closure, quadrature signal input, motor output signal generation, on-the-fly changes, commutation and much more. Additional features include S-curve, trapezoidal, velocity contouring, electronic gearing and user-generated profile modes. The cards accept input parameters such as position, velocity, acceleration and jerk from the host, and generate a corresponding trajectory. Prices start at \$380 in OEM quantities.

Performance Motion Devices, Lincoln, MA. (781) 674-9860. [www.pmdcorp.com].

VXS Card Blends Dual Core PowerPCs, Dual FPGAs

A backward-compatible successor to VME, the VXS continues to grow its ecosystem. Adding to the mix is a DSP processing card that integrates a Freescale MPC8641D processor, two Xilinx Virtex-5 FPGAs and a VXS-based high-speed serial interconnect fabric. Called the VPF2 from VMETRO, the board tackles both high-bandwidth preprocessing and demanding back-end processing in one 6U VME64/VITA 41 product for advanced DSP applications such as real-time video processing, surveillance, radar and others that demand the extremely high levels of flexibility and performance.



The processing heart of the Phoenix VPF2 is a Freescale MPC8641D dual-core processor based on Power Architecture technology. The cores run up to 1.25 GHz with 2 Gbytes of memory to support operating systems such as VxWorks and Linux. Integrated within the MPC8641D processor is a complete I/O subsystem, including two Gigabit Ethernet ports, serial I/O, dual DDR/DDR2 memory controllers, VME interface and independent x8 PCI Express links to the Xilinx FPGAs and the XMC/PMC site. The VPF2 has Ethernet options that support both RJ45 and optical interfaces or backplane I/O. The VPF2 will be available in a number of environmental build options ranging from air-cooled commercial to rugged conduction-cooled.

VMETRO, Houston, TX. (281) 584-0728. [www.vmetro.com].

FPGA DSP Devices Target Low-Power Designs

The portable, handheld segment ranks as one of the most dynamic segments of military system design. DSP-capable FPGAs are vital to such devices. The Spartan-3A DSP platform from Xilinx offers 20 GMACs of DSP capability. The Spartan-3A DSP platform is part of the Xilinx XtremeDSP solutions that provide developers with a complete portfolio of programmable logic devices, IP, development tools and a third-party DSP ecosystem.



The platform is based on Xilinx's Spartan-3 generation FPGAs, with the added power management and connectivity features of the Spartan-3A platform. At the heart of the Spartan-3A DSP architecture is the XtremeDSP DSP48A slice that enables designers to implement many independent arithmetic functions. The XtremeDSP silicon portfolio delivers three device platforms: the Virtex-4 SX platform with over 250 GMACS at 500 MHz, Virtex-5 SXT platform for ultra high bandwidth with over 350 GMACS at 550 MHz and integrated low-power serial connectivity, and the Spartan-3A DSP platform with over 30 GMACS at 250 MHz. The 3SD1800A device is priced at \$29.85 and the 3SD3400A device is priced at \$44.95. Pricing is for 25,000 units in volume production, end 2008.

Xilinx, San Jose, CA. (408) 559-7778. [www.xilinx.com].

Mini-ITX Mainboard Sports Dual-LAN, Dual-LVDS

Redundant networking and I/O links are a good way to ensure robust and reliable operations. A new Mini-ITX mainboard from VIA Technologies based on the VIA CX700 system media processor incorporates a number of features for the x86-based embedded market, such as greater device performance, clearer definition video and storage technologies, and an I/O set including two LAN ports and native support for two LVDS panels, four COM ports, a PCI slot and up to six USB 2.0 ports. Project-based customers also have the option of a VIA CX700M2 version with added TV-out functionality.

Incorporating the ultra-low-power consumption VIA C7 processors at 1.5 GHz or fanless at 1 GHz, the VIA EPIA LT-Series platform provides high performance per watt and a feature set dedicated to connectivity. Supporting up to 1 Gbyte of 533 MHz DDR2 memory, the VIA CX700 drives a range of connection options including dual LVDS support and two 10/100 fast Ethernet modules, with a Gigabit option, two SATA connectors and up to six USB 2.0 ports. The VIA EPIA LT Mini-ITX mainboard is compatible with Microsoft Windows 2000/XP, XPe, CE and Linux, as well as being fully compatible with all Mini-ITX, FlexATX and MicroATX chassis and associated accessories.

VIA Technologies, Fremont, CA. (510) 683-3300. [www.via.com.tw].



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VME Card Synchronizes 2 GHz A/D Modules

Software Defined Radio and similar applications seem to have an endless appetite when it comes to speedy A/D conversion. Supporting those needs, Pentek offers a 2.2 GHz clock, synch and gate distribution board for synchronizing multiple I/O modules, which facilitates sampling and timing for a wide range of multichannel, high-speed data acquisition, DSP and software-radio applications. Configured as a 6U VME board, the Model 6890 synchronizes up to eight modules, each receiving a common clock up to 2.2 GHz along with timing signals for synchronizing, triggering and gating functions. The Model 6890 currently supports Pentek's Model 6826 Dual 2 GHz, 10-bit A/D Converter VME board.

Developed specifically to address the critical timing needs of synchronous multichannel data acquisition and DSP systems, the Model 6890 board simplifies system integration tasks. For example, when combined with eight Model 6826 Dual-Channel 2 GHz, 10-bit A/D Modules, the resulting system provides 16 A/D converters all sampling at 2 GHz, plus eight FPGAs with a total of 352,000 programmable slices and 800,000 logic cells. Pricing for the Model 6890 starts at \$4,995. The single-channel version of the Model 6826 starts at \$19,345.

Pentek, Upper Saddle River, NJ. (201) 818-5900.
[\[www.pentek.com\]](http://www.pentek.com).

Data Acq Card Outputs Have Isolated Grounds

Military data acquisition and test used to require racks of boards for any sophisticated system. Today the same functionality is availing in PC-compatible solutions. A new data acquisition processor (DAP) board can eliminate two serious potential problems—ground currents and phase errors—from analog outputs in applications. The MSXB 076 from Microstar Laboratories includes eight single-ended analog outputs with an isolated ground for each output. Eight boards in a 19-inch rack-mountable industrial enclosure can connect to a single DAP board. Multiple DAP boards can work together in a PC and across a network as a synchronized system.

MSXB 076 boards slot into a backplane in a standard industrial enclosure like other signal-conditioning products that conform to the external hardware specifications of the Microstar Laboratories channel architecture. A backplane connector on each board connects it to a digital backplane factory-fitted into the industrial enclosure. An interface board that also plugs into the backplane receives digitized waveforms from a DAP board in a PC. DAP boards communicate among themselves independently of Windows to synchronize their clocks with one another. They then all work synchronously as a networked data acquisition system. The MSXB 076 board is priced at \$695.

Microstar Laboratories, Bellevue, WA. (425) 453-2345.
[\[www.mstarlabs.com\]](http://www.mstarlabs.com).



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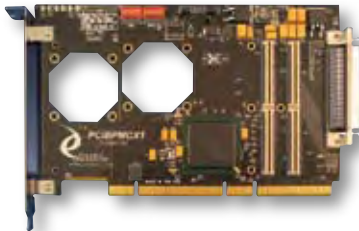
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Adapter Puts PMC into Standard PCI/PCI-X Slot

PCI is arguably the most successful bus to invade the embedded market, with numerous flavors and form-factors for every need. Dynamic Engineering's latest PCI-X product is the PCIBPMCX1, an adapter/carrier converter card that provides the ability to install one PMC card into a standard PCI/PCI-X slot. The PCIBPMCX1 PMC card slot can be programmed for 3.3 or 5V operation by the user, and the primary PCI bus implementation is universal voltage. It is suitable for PCI or PCI-X operation with 32-bit or 64-bit data and 33, 66, 100 or 133 MHz clock. The PMC user I/O connector Pn4 is available on a SCSI II connector.



The PCIBPMCX1 has a cooling cutout for increased airflow to the PMC. A cutout is preferred over a fan mounted to the PMC adapter for several reasons including: many components are not shielded against close proximity to electromagnetic fields, and the reduction in MTBF that an additional mechanical device represents. The PCI bus is interconnected to the PMC via a 64-bit 133 MHz-capable bridge. The bridge allows the PCI bus to operate with different parameters than the PMC card. Single unit price is \$625 and quantity discounts are available.

Dynamic Engineering, Santa Cruz, CA.
(831) 457.8891. [www.dyneng.com].

PMC Serves up 10 Mpolygons/s 3D Graphics

Military graphics subsystems are riding the wave of sophisticated graphics silicon created



for the gaming industry. Built around the Carmine MB86297 GPU, the third generation of high-end graphics products developed by Fujitsu, a new graphics PMC provides multiple features including geometry processing for 2D/3D

graphics, pixel processing hardware and video capture. The IC-GRAMCa from ACT/Technico is an IEEE 1386-compliant PMC that also offers 3D performance of up to 10 Mpolygons/s, the highest rendering performance available in the embedded market, with the lowest power consumption.

The IC-GRAMCa features a 128 Mbyte DDR memory at 266 Mb/s, two video output channels with resolutions of up to 1280 × 1024 pixels at 60 Hz and multiple interfaces (DVI, VGA, RGB, STANAG). Each digital video output port allows transparent processing, such as an overlay display up to eight layers and alpha planes for four layers. The IC-GRAMCa has a DVI 1.0-compliant digital interface or a VGA-compatible interface. The VGA interface can be routed on the DVI-I connector or PN4 I/O connector through a video multiplexer. Pricing starts at \$2,500 per unit. A conduction-cooled version is also available.

ACT/Technico, Warminster, PA.
(215) 956-1200. [www.acttechnico.com].



Celeron M PCI-104 Card Withstands HALT

Highly Accelerated Life Testing (HALT) is fast becoming the litmus test for finding the potential weak links in a product design and to determine the true operating and destruct limits. Ampro Computers has put its CoreModule 800 SBC through HALT processes. The company reports that the CoreModule 800 withstood intense multi-axis vibration of 50Grms while operating over a very broad operating temperature range of -60° to +90°C. This compact embedded computer sports a 1 GHz Intel Celeron M 373 processing into the tiny PCI-104 form-factor standard without protruding beyond the required 3.6 x 3.8-inch board outline.

The CoreModule 800 contains a rich set of PC-compatible subsystems, including DDR 333 SODIMM up to 1 Gbyte, USB ports, serial ports, Gbit Ethernet, an IDE channel and AMI BIOS with support for optional MiniModule ISA PC/104-Plus bridge card for compatibility with the hundreds of off-the-shelf PC/104 and PC/104-Plus modules. The 1 GHz CoreModule 800 is on the shelf and available immediately. The CoreModule 800 QuickStart Kit includes device drivers and Board Support Packages (BSPs) for Windows XP, Windows XP Embedded, Windows CE, QNX, VxWorks and a full Linux 2.6 distribution. The price is around \$1,000 for moderate production volumes.

Ampro Computers, San Jose, CA. (408) 360-0200. [www.ampro.com].



PC/104-Plus/Express SBCs Boast Full Temp Range

PC/104 is entrenched as a favorite form-factor in space-constrained military applications. A new single board computer line for highly demanding, embedded applications from Fastwel is designed in PC/104-Plus (CPC1600) and PC/104-Express (CPC1700) formats. The boards feature Intel Pentium M processors up to 2.0 GHz and with a 533 MHz front side bus.

The 82915GM Chipset and ICH6 dual-channel memory interface provide for access to up to 1 Gbyte of PC4200 DDR2. A conduction-cooling solution provides effective heat dissipation from CPU and GMCH to external enclosure to ensure fan-free operation through the full industrial temperature range of -40° to +85°C. All components including CPU and memory are soldered on board to provide reliability in high shock/vibration environments.

A video system supports two independent displays, CRT or flat panel and an LVDS interface; resolution is up to 2048 × 1536. Peripheral devices can be connected to the boards through four high-speed USB 2.0 channels. Input/output capabilities can be expanded by means of additional features: for CPC1600 a 32-bit, 33 MHz (3.3/5V) PCI interface, for CPC1700 a x4 PCI Express interface. Additional reliability of CPC1600 and CPC1700 is provided by a hardware monitoring subsystem, watchdog timer and reserved copy of BIOS in CMOS memory.

Fastwel, Brooklyn, NY. (718) 554-3686. [www.fastwel.com].

Gbit Ethernet Switch/Router Climbs Aboard 6U VPX



VPX, the fabric-based next-gen VME form-factor is gaining more and more momentum every month. A variety of SBC products have emerged, and now special function boards like Ethernet switch boards are adding to the VPX ecosystem. For its part, Curtiss-Wright Controls Embedded Computing has announced the first high-density 6U VPX Gbit Ethernet

multilayer switch/router board designed for rugged embedded aerospace and defense applications.

The new VPX6-684 FireBlade II, available with 12, 20 or 24 Gbit Ethernet ports and up to 4x10 Gbit Ethernet ports, is ideal for system integrators architecting secure high-performance IPv4/v6 Intra-Platform Networks (IPNs). The board, which operates as either a fully managed or an unmanaged switch/router, provides significant performance and configuration advantages to developers building Layer 2 or Layer 2/3+ networks. Additional feature enhancements include support for routing up to 4x10 Gbit Ethernet to the FireBlade's P1 connector, and support for copper interfaces to the backplane for all of the board's 12, 20 or 24 Gbit Ethernet ports.

Curtiss-Wright Controls Embedded Computing, Leesburg, VA. (703) 779-7800. [www.cwembedded.com].

6U cPCI Board Monitors System from Remote PC

CompactPCI has earned its stripes in the military market. With nearly 15 years of maturity under its belt, the technology ranks as a low-risk choice for military system designers. A new 6U CompactPCI (cPCI) System Monitoring and Control Board from One



Stop Systems monitors the health and status of chassis systems, making it suited to any military comms installation that requires monitoring of critical system parameters.

The 6U SYSMON II installs in the system enclosure and communicates to a remote PC via a 100Base-T Ethernet connection. It monitors eight fan tachs, eight temperature sensors, up to eight voltages and eight inputs and eight outputs. All configuration parameters are stored in non-volatile flash. The 6U SYSMON II provides a complete system package for applications requiring continuous operating computing. It lists for \$1,280 and is available immediately as part number OSS-CPCI-6U-SYSMON2.

One Stop Systems, Escondido, CA. (760) 745-9883. [www.onestopsystems.com].



Straight Talk
Engineer to Engineer

Intel Processors...Low Power?? Yes!

Hello Everyone! Sprechen Sie talk? It's me, Martin, again for our September's installment of Martin's Corner.

This month I want to touch on the fact that Intel processors are getting to be very attractive in the low power space (so much so that you could never fry an egg on one).

We, at Corvalent, are excited by the new Low Power and Ultra Low Voltage Intel processors that are hitting the market. If you are privy to Intel's roadmaps, you know what we're talking about. Some solutions are now in the five watt range with likely even lower wattages next year. This means that designs that used to only be passively cooled X-Scale candidates are now able to utilize Intel Architecture (IA). These processors will be ideal for medical, security & surveillance, oil & gas, point-of-sale, aerospace, and military/defense applications, to highlight a few.

The good thing about this is that all the tools and software that have been written for IA will now be able to be utilized by us as a system integrator and by our customers who have many of their applications written for IA.

Some of the processors we are excited about include:

- Intel® Core™ Duo Processor ULV
- Intel® Celeron® M Processor ULV
- Intel® Core™ 2 Duo Processor Low Power

For more information on Intel's future Ultra Low Voltage processors visit: www.intel.com/design/embedded

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Coming Next Month

- **SPECIAL SECTION: Vetronics (Vehicle Electronics).** The sophistication of onboard communications and control electronics is expected to multiply for both next-generation and Current Force fighting vehicles. All that is putting pressure on system designers to find ways to meet the trickier cooling, shock and vibration problems that emerge when more computing gear is packed into those vehicles. This section looks at those developments as well as the technologies and solutions critical for vetronics. Included will be an update on the Army's Future Combat Systems program and Current Force upgrades that interrelate with that program.
- **Military-Specific I/O.** Tried and true I/O schemes, such as MIL-STD-1553 and ARINC 429, remain popular for pure control applications. But they're bandwidth-limited by today's standards. A slew of multipurpose communications protocols provide options to suit emerging needs. Articles in this section compare today's crop of I/O schemes relevant to military users.
- **Mezzanines in the Military.** Military system designers love to think in modular blocks. That's why mezzanine technologies rank among the key product areas embraced by military integrators. Articles in this section examine the latest mezzanine choices such as XMC and AMC, with a look at developments in established mezzanine flavors such as PMCs.
- **Fibre Channel Boards.** Fibre Channel boasts proven success in commercial markets along with a solid set of mature specifications and standards, with work on going toward higher performance levels. Fibre Channel remains popular as a back-end link to storage in radar, SIGINT and other military systems. It's seen as a "here today" alternative like switched fabric storage links. This Tech Focus section updates readers on Fibre Channel boards in PMC and other form-factors, and provides a product album of representative boards.





Editorial

Jeff Child, Editor-in-Chief



Dr. Truchard's Time Machine

I can't help it. Each time I meet with folks at National Instruments I get the distinct feeling that NI's cofounder, president and CEO, Dr. James Truchard, secretly invented a time machine a couple decades ago. How else to explain why the company is today aligned so perfectly with technology trends in processing, form-factors and fabric interconnect technologies? Clearly Dr. Truchard must have—using LabView no doubt—designed a time machine, looked ahead to 2007 and planned the company's strategy accordingly. That feeling surfaced again last month when I visited the company's headquarters in Austin.

All jesting aside, the reason NI is benefiting so successfully from the direction in serial fabric interconnects and embedded computing technologies are because an overall trend in the test and instrumentation market. There was a time when complex military embedded systems, and aircraft in particular, couldn't get through its development phase without bringing to bear heavy-duty test and instrumentation equipment. Today such systems can be pieced together around standard and embedded computer systems. Once that meant large racks of boards—based on VXI and other older form-factors. Now the same test functions can be done on the PC using USB, PCI Express data acquisition and test modules. And the PC itself—in desktop, laptop or single board embedded computer form—functions as the platform for running the test software and to serve as user interface.

Recent marriages of standard form-factors have further enhanced the performance and modularity available for these applications. CompactPCI and PCI Express have blended into the emerging CompactPCIe. And CompactPCIe has in turn been adopted as the basis for the new version of the PXI instrumentation standard, called PXI Express. This standard allows CompactPCIe boards to be used with instrumentation-specific boards that have additional timing and trigger lines defined.

As the PC shifts into the role of preferred military/aerospace test platform, the result is not only more integrated, less costly systems, but also more mobile systems. When a complex, real-time data acquisition system is small enough to fit in the back of a truck or Humvee, suddenly a whole range of new capabilities open up.

During my visit to NI, their engineers described a couple examples along those lines. One is part of the Quiet Technology Demonstrator 2 (QTD2) project where Boeing flight-tested new technologies intended to reduce the amount of noise aircraft generate. During the first stage of the QTD (QTD1) project in 2001, Boeing deployed a VXI test system that was limited in both channel count and channel bandwidth. The system required a centralized data architecture that required them to co-locate all the VXI chassis for synchronization, necessitating long cable runs from the

microphones to the data acquisition system. That meant about 10 miles of cable per 100 channels of data acquisition. On top of that there were other challenges including time delays when synchronizing instruments across multiple VXI chassis. That meant significant cost per channel, and significant time required for data retrieval.

In contrast, the recent QTD2 phase of the project made use of the flexibility and modularity of PXI to create a scalable system with virtually unlimited channel-count capability. By taking advantage of NI's timing and synchronization cards, the Boeing engineers could distribute the data acquisition hardware into the microphone array, decreasing cabling by nearly 80 percent while maintaining within one degree of phase match between channels. The controller cards were each linked through Gbit Ethernet to one central host computer. That enabled faster post-acquisition data recovery to the host computer and other systems used for data processing and analysis. This unlimited, distributed architecture reduced the cost per channel by more than 50 percent compared to the previous system.

Another example, although not military in nature, is the testing of cell phone and other types of RF handsets in a regional area. Traditionally, when a new handset was designed it was necessary to take the prototypes, and for example, drive around the city of Chicago and see how the handsets functioned. Now the electronics to do sophisticated RF signal capture hardware link to real-time streaming data storage can be implemented in a portable, PXI-based system small enough to ride in the back of a truck.

That means instead of testing each individual new handset prototype, engineers drive around just once and capture the complete RF spectrum in a particular region and store it in a disk. That data set—"RF Spectrum in Chicago in Spring" for instance—can then be brought back to the lab and used to test handsets functionality using the stored RF spectrum data. The same concept, obviously, could work for developing military Software Defined Radio handsets—capturing the complete RF Spectrum of "Baghdad in the Summer" for example, and bringing it back to the lab to test against.

By riding this wave of PC-based technologies, National Instruments is today in position with all the critical PCI Express, PXI, CompactPXIe and USB products that make up the new paradigm for advanced test and instrumentation systems, with its LabView software supporting them all. Well, Dr. Truchard, next time I visit your offices in Texas, please let me peek into that back room where you keep your time machine. I'm dying to know what's on deck for 2017. ■■

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